

# **LOW POWER DYNAMIC COMPARATOR DESIGN**

*A Thesis submitted in partial fulfilment of the Requirements for the degree of*

Master of Technology

In

Electronics and Communication Engineering

Specialization: VLSI Design & Embedded System

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## Certificate

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This is to certify that the work in the thesis entitled “**Design of low power dynamic comparator**” by **Prasanta Kumar Senapati** is a record of an original research work carried out by him during 2013 - 2014 under my supervision and guidance in partial fulfilment of the requirements for the award of the degree of Master of Technology in Electronics and Communication Engineering (VLSI Design & Embedded System), National Institute of Technology, Rourkela. Neither this thesis nor any part of it, to the best of my knowledge, has been submitted for any degree or diploma elsewhere.

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- b) The work has not been submitted to any other Institute for any degree or diploma.
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**Prasanta Kumar Senapati**

**28<sup>th</sup> May 2014**

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# **ABSTRACT**

In many applications there is a growing demand for the development of low voltage and low power circuits and systems. Low power consumption is of great interest because it increases the battery lifetime. One of the main building blocks in many applications is the analogue-to-digital converter (ADC) which serves as an interface between the analogue world and the digital processing unit. In all these designs the comparator of the ADC, which is one the most power hungry blocks, is always on. In order to reduce the power consumption of the ADC it is possible to turn the comparator off when the decision is made and the comparator is not needed until the next clock cycle. This work provides a comprehensive review about a variety of comparator designs - in terms of performance, power and delay. The initial part of the work was working with static comparators architectures with different pre-amplifier modifications .Later part deals with two dynamic comparator architectures. The main components of such comparators are the preamplifier and latch circuit. Preamplifier is used for removing the kickback noise and the dc offset voltage while the latch is required for the comparison. The proposed architectures operate on three phases which are non-overlapping and dissipate  $7\mu\text{W}$  power when operated on a single 1V supply voltage. The latch is basically a back to back connected inverter circuit which inactivated only during the second phase.

# **MOTIVATION**

With the rapid growth of electronics industry mostly portable electronics systems, such as wireless communication devices, consumer electronics or battery-powered medical devices where the battery life is very important. The demand for developing low voltage and low-power circuit techniques for these type of devices and building blocks is very essential now. With the trend that A/D interfaces are considered as a important part in ICs containing mostly digital blocks for DSP and control, the use of the same supply voltage for both analog and digital circuits can reduce the overall system cost by eliminating the need of using multiple supply voltages. Avoiding higher supply voltages and thicker oxide transistors also helps in reducing IC costs. Therefore, in order to be compatible with low-voltage devices a new generation of A/D converters are required. A major component of an A/D block is the Comparator, which consume maximum power. A better design of low power comparator in general reduces the AD/DA converter cost. In general, low-voltage circuit design is desirable to reduce the number of battery cells for reasons of low weight and small system size.

## Literature survey:

- D. lackuline Moni and P. lisha[1]

In this paper for a given vdd the power dissipation of different types of CMOS latch comparators are compared at and delay and Power Delay Product of the different comparators were found. Simulation results were get that shows power Consumption of the dynamic latch comparator with inverter is less compared to other type of comparators

- Riyan Wang , Kaihang Li, Jianqin Zhang, Bin Nie[2]

A novel CMOS comparator suitable for high speed pipeline ADCs is presented in this paper. In the proposed architecture, the first stage is designed to be rail-to-rail input range preamplifier. The samplers and self-biased post-amplification make up of output stage, which significantly speeds up the comparison rate. The designed comparator presents promising and good optimized performance in term of speed and resolution. Simulation results show that this comparator achieve the resolution of 1mV, with the latch clock of 100MHz.

- Shabi Tabassum, Anush Bekal, Manish Goswami[3]

This paper concludes the preamplifier positive feedback latch based comparator design. The proposed design is implemented using 180nm CMOS technology, dissipates 70 $\mu$ W power when applied single 1V power supply

- Sandeep K. Arya, Neel Kamal[4]

The circuits studied and simulated in this paper are Preamplifier dynamic latch circuit that consists of a preamplifier followed by a double regenerative dynamic latch and the Buffered dynamic latch circuit that consists of a basic dynamic latch comparator followed

by an inverter Buffer stage. The power dissipation of preamplifier latch and buffered latch comparator operating at frequency 160 MHz and 100 MHz are 960.129  $\mu$ W And 1.132 mW respectively.

- Ali Valaeea and Mohammad Maymandi-nejad[5]

A 9-bit ultra-low power switched-comparator SA-ADC is presented in this paper. The proposed SA.ADC can operate with a supply voltage of as low as 0.5V in 0.18  $\mu$ m CMOS technology.

- [6][7][8][9] In these book basic structures of comparators along with component are explained. Basic design techniques of components are given and sizing issues are discussed. Comparators basic parts are covered along with their role in ADC and DAC



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# **CHAPTER 1:**

## ***INTRODUCTION***

In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less hysteresis, less Offset voltage are required is Analogue to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators.

In this literature keeping in mind that resolution is inversely proportional to the DC gain of the amplifier, different type of preamplifier has been designed in order to achieve the gain and the resolution. Very little emphasis is placed on actual details of operation of these structures along with experimental results to compare offset values, power consumption, and speed of different structures. These experimental offset values vary from 18mV to 50 mV. However, the literature is devoid of any information on how other non-idealities such as imbalance in parasitic capacitors, common mode voltage errors or clock timing errors effect these structures

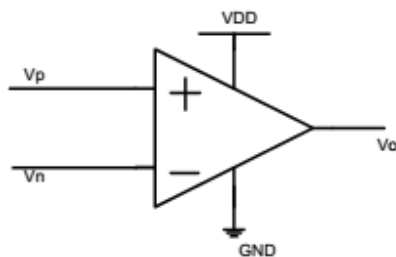
## 1.1 BASIC CMOS COMPARATOR:-

The basic operation and the schematic symbol of a voltage comparator are shown in fig1.1, this comparator can also be considered as a decision making circuit.

### Definition:-

The comparator is a device which compares an analogue signal with another signal or reference and outputs a binary level (signal 0 or 1) based on the comparison.

If the positive terminal voltage  $+V_P$  of the comparator is greater potential than the  $-V_N$ , the input to the negative terminal, the output of the comparator will be a logic 1, In other hand if the  $+$  input is less than the  $-$ input then the output of the comparator will be logic 0.



$$V_P < V_N \text{ then } V_O = V_{SS} = \text{logic 0.}$$

$$V_P > V_N \text{ then } V_O = V_{DD} = \text{logic 1.}$$

Fig. 1.1: Comparator operation

What is meant here by an analogue signal is one that can have any of a continuum of amplitude values at a given point in time. In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region. The comparator is widely used in the process of converting analogue signals to digital signals. In the analogue-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analogue signal. In its simplest form, the comparator can be considered as a 1-bit analogue-digital converter.

The Presentation on comparators will first examine the requirements and characterization of Comparators. It will be seen that comparators can be considered as open-loop and regenerative comparators. The open-loop comparators are basically op amps without

compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.



# **CHAPTER 2:**

## **FUNDAMENTALS OF COMPARATOR DESIGN**

## 2.1. CHARACTERISATION OF COMPARATOR:-

A positive voltage applied at the  $V_p$  input will cause the comparator output to go positive, whereas a positive voltage applied at the  $V_n$  input will cause the comparator output to go negative. The upper and lower voltage limits of the comparator Output are defined as  $V_{OH}$  and  $V_{OL}$  respectively.

### 2.1. A. Static Characteristics:-

A comparator defined above is a circuit which has a binary output whose level is established on a comparison of 2 analog inputs. Which is illustrated in Fig.2.1 As shown in this figure? The output of the comparator is high ( $V_{OH}$ ) when the difference between the non inverting and inverting inputs is positive, and low ( $V_{OL}$ ) when this difference is negative. Even though this type of behaviour is impossible in a real-world situation, it can be modelled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Fig.2.2 comprises a voltage controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the

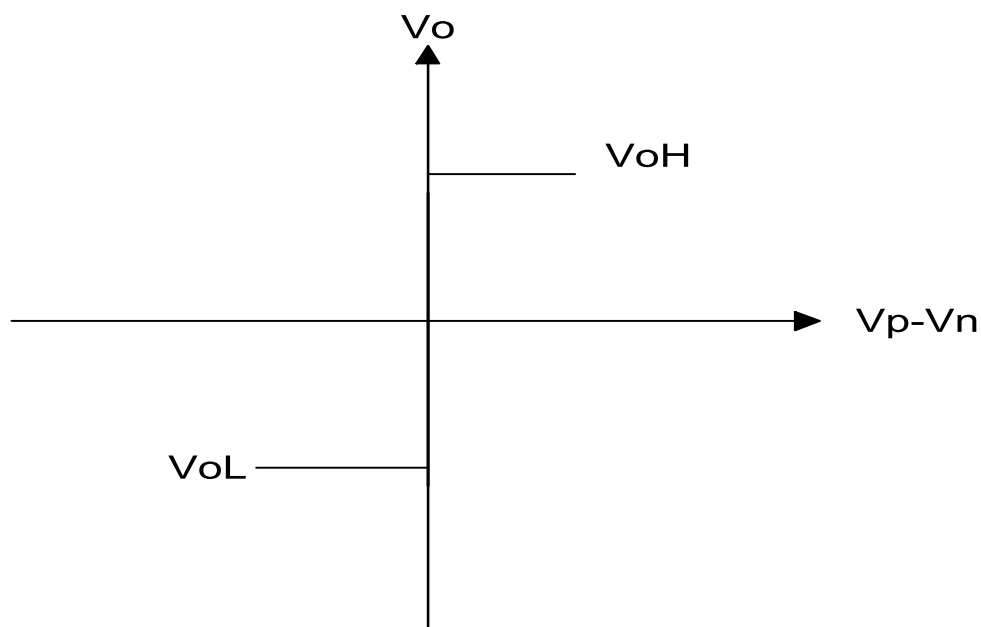


fig 2.1.A.(i) ideal transfer curve of a comparator

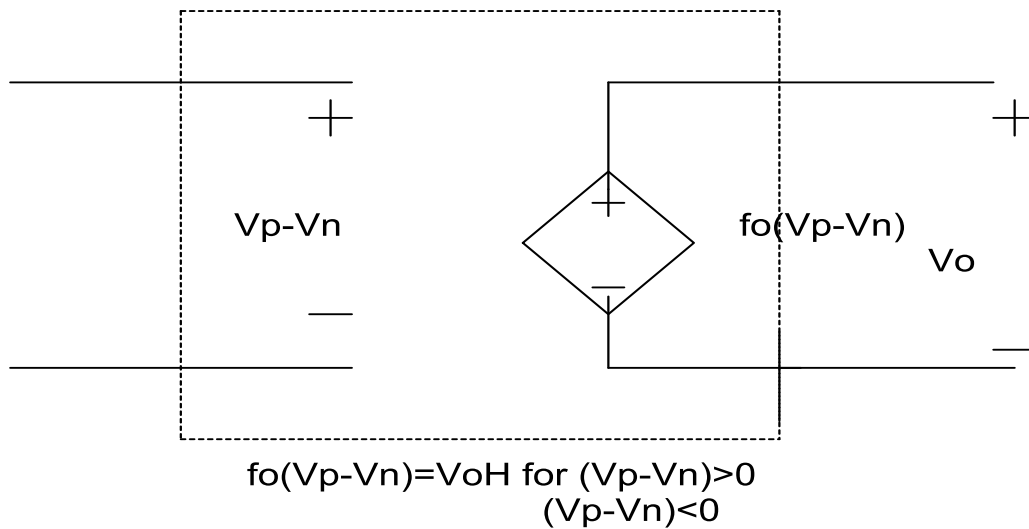


fig 2.1.A(ii): model for an ideal comparator

The second non-ideal effect seen in comparator circuits is input offset voltage,  $V_{os}$ . In Fig. 2.1 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value  $+V_{os}$ , then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit [1] for a given design. Figure 2.4 illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Fig. 2.5. The  $\pm$  sign of the offset voltage accounts for the fact that  $V_{os}$  is unknown in polarity.

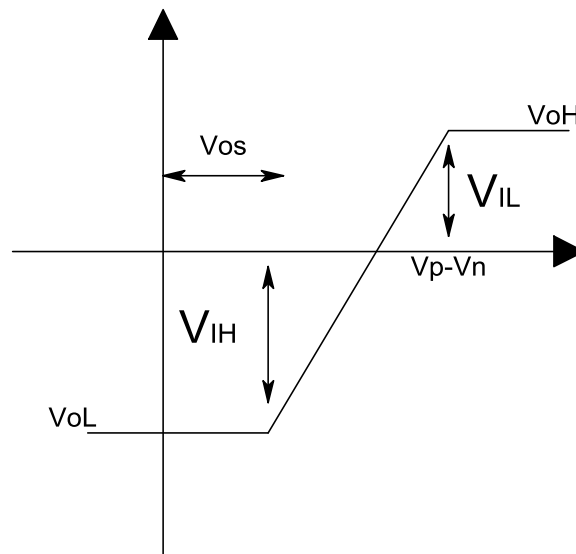


fig2.1.A(iii): transfer curve of a input offset voltage

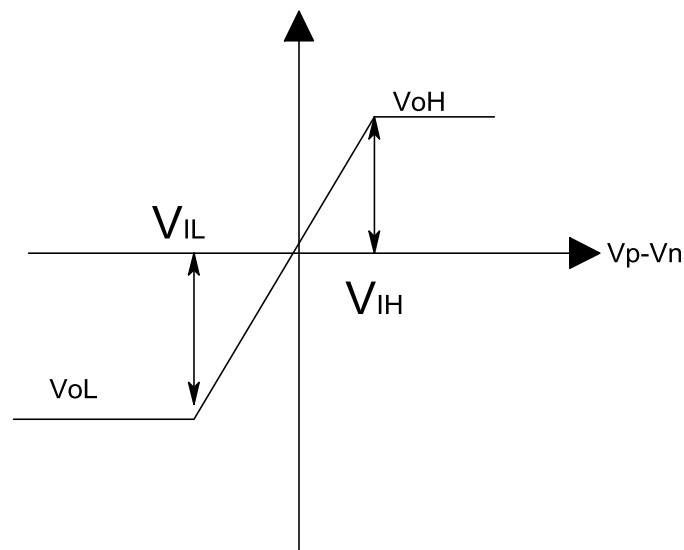


fig2.1.A(iv): transfer curve of a comparator with finite gain

All these characteristics can be modelled in the same manner as was done for the op- amp. Because the input to the comparator is usually differential, the input CM-range is also significant. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally.

This input CM- range is commonly the range where all transistors remain in saturation level. Though the comparator is not designed to operate in the transition region among the two binary output conditions, noise is still vital to the comparator. The noise of a comparator is

demonstrated as if the comparator were biased in the transition span of the voltage-transfer characteristics.

The noise will create to an uncertainty in the transition state as shown in Fig.2.6. The uncertainty in the transition state will lead to jitters or noise in the circuits where the comparator is working.

## 2.1. B.Dynamic Characteristics:-

The dynamic characteristics of the comparator comprise both small and large-signal behaviour. We do not know, at this point, how long it takes for the comparator takes to respond to the differential input. The characteristic delay between input and output state is the time response of the comparator. The response of a comparator to an input is a function of time. There is a delay between the input signal and the output signal. This time difference is called propagation delay of comparator

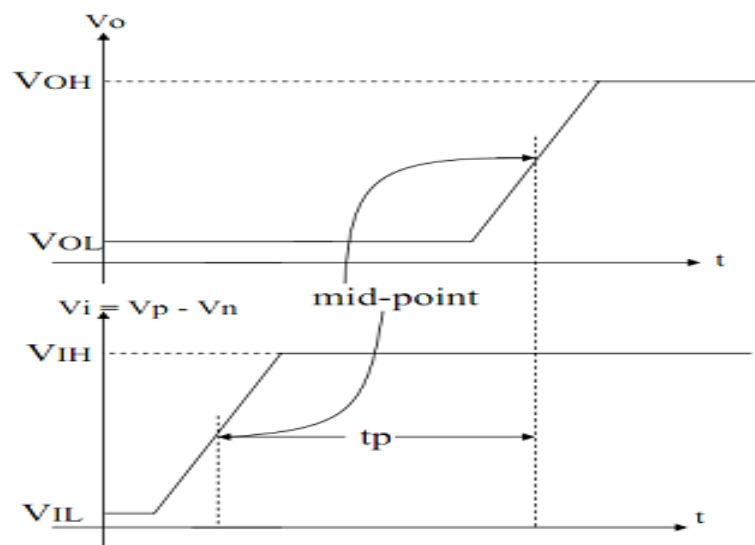


Fig.2.1.B-propagation delay

## Slew Rate:

Slew rate is defined as the rate of change of output voltage with respect to time.  $SR = dV_{out} / dt$

If the rate of rise and fall of a comparator becomes very large, the dynamics may be restricted by the slew rate. SR comes from the relationship,  $I = C \, dV/dt$  where  $I$  and  $C$  are the current and capacitor voltage across a capacitor. If the current becomes less, then the voltage rate becomes less. So for a comparator that is SR limited we have,  $T_p = \Delta T = \Delta V / SR = (V_{OH} - V_{OL}) / 2 \cdot SR$  where  $SR$  = slew rate of comparator.

# **CHAPTER 3.**

## **BLOCK DIAGRAM OF VOLTAGE COMPARATOR**

### 3.1 comparator block diagram

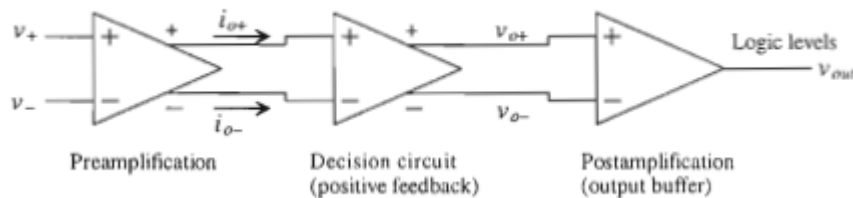


Fig-3.1: comparator block diagram

The block diagram of a high performance comparator is shown in above figure. It has 3 stages

- (i) input pre amplifier,
- (ii) A positive feedback or decision stage
- (iii) An output buffer.

In preamplifier amplifies the input signal to increase the comparator sensitivity and isolate the signal input of the comparator from the kickback noise from the positive feedback stage.

In the positive feedback block the determination of the larger input signal is determined. The output buffer gets input from decision circuit and amplifies this signal and outputs a digital level either 0 or 1. Designing of comparator takes care of comparator gain, common mode range, propagation delay and power dissipation,



### 3.2 Comparator schematic

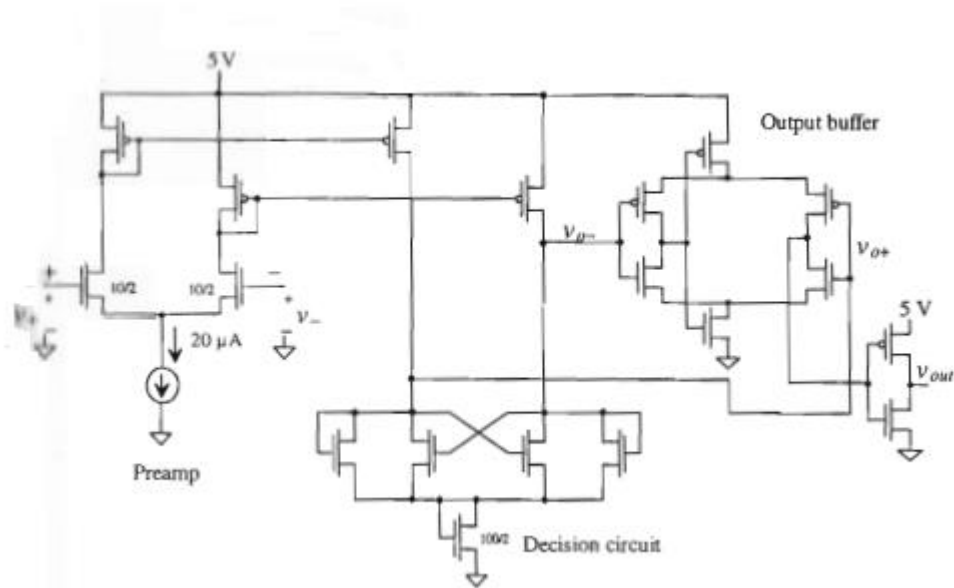


Fig 3.2-schematic of comparator

### 3.3 Pre amplification stage:-

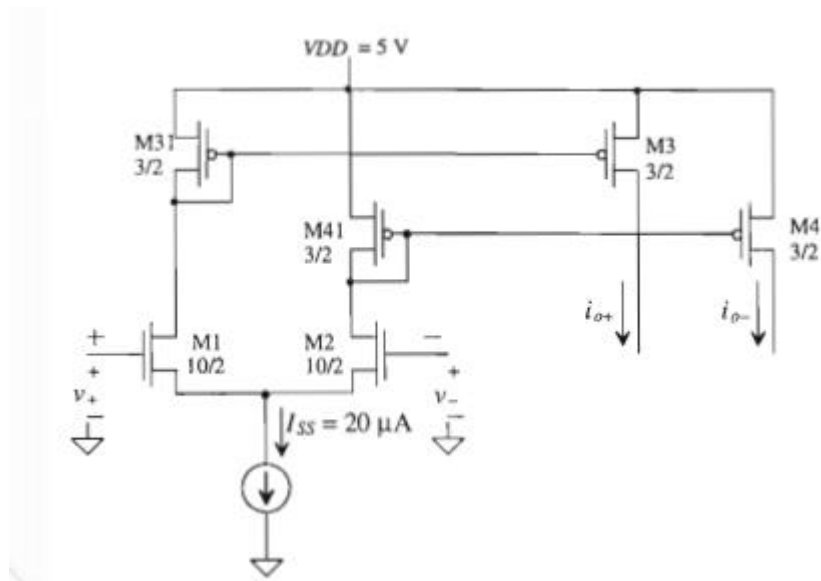


Fig 3.3-preamplifier of comparator

The pre-amplifier stage is a differential amplifier with active load.

The trans-conductance determines the gain of the stage.

### 3.4 Small signal analysis:

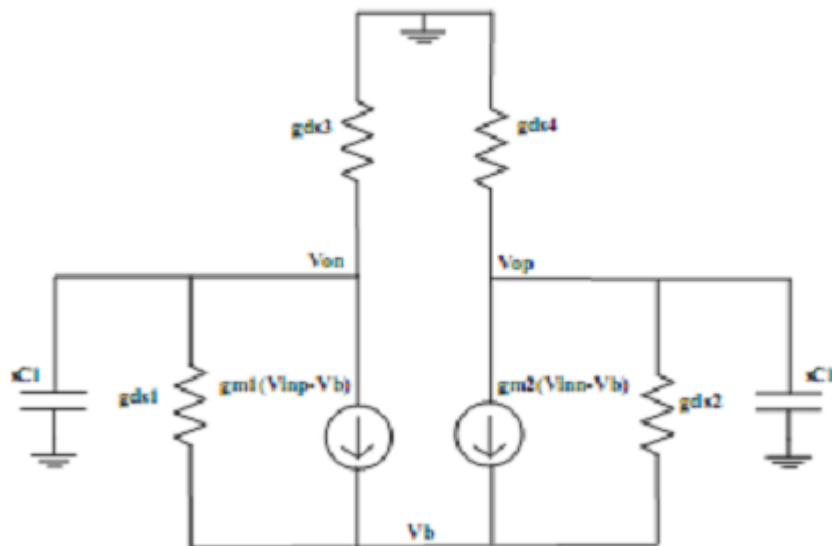


Fig 3.4-small signal analysis

The DC gain can be written as:

$$A_v = \frac{g_{m1}}{g_{ds1} + g_{ds3} + sC1}$$

$$A_v = \frac{g_{m1}}{g_{ds1} + g_{ds3}}$$

As shown in the figure taking the W/L ratio 10/2 and Iss= 20uA

$$i_{o+} = \frac{g_m}{2}(v_+ - v_-) + \frac{I_{ss}}{2} = 20\mu A - i_{o-}$$

$$g_m = g_{m1} = g_{m2} = 71\mu A/V$$

To further increase the gain we can resize the width of M3 and M4 relative to M31 and m41 .

### 3.5:DECISION CIRCUIT:-

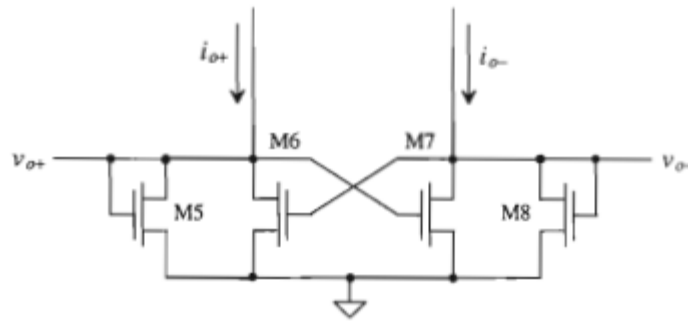


Fig.3.5.a. decision circuit

discriminating mV level signals. The circuit used in the present comparator uses positive feedback from the cross gate connection of M6, M7 to increase the gain of the decision. The decision circuit is the heart of the comparator and should be capable of element

Let us assume  $i_{O+}$  is larger than  $i_{O-}$  then M5 and M7 are on and M6 and M8 are off. we will assume that  $\beta_5 = \beta_8 = \beta_A$  and  $\beta_6 = \beta_7 = \beta_B$

$$V_{O+} = \frac{\sqrt{2 i_{O+}}}{\beta_A} + V_{thn}$$

$$V_{O-} = 0V$$

If  $i_{O-}$  increases and  $i_{O+}$  decreases switching takes place when  $V_{ds}$  of M7 =  $V_{thn}$  of M6.

At this point M6 starts conducting

$$\text{Current through M7} = I_{O-} = \frac{\beta_B}{\beta_A} \cdot I_{O+}$$

$$\text{The switching point voltage } V_{sph} = V_+ - V_- = \frac{I_{ss}}{gm} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \text{ and } V_{spl} = -V_{sph}$$

$V_{sph} = V_{spl}$  is the minimum difference between  $V_{O+}$  and  $V_{O-}$

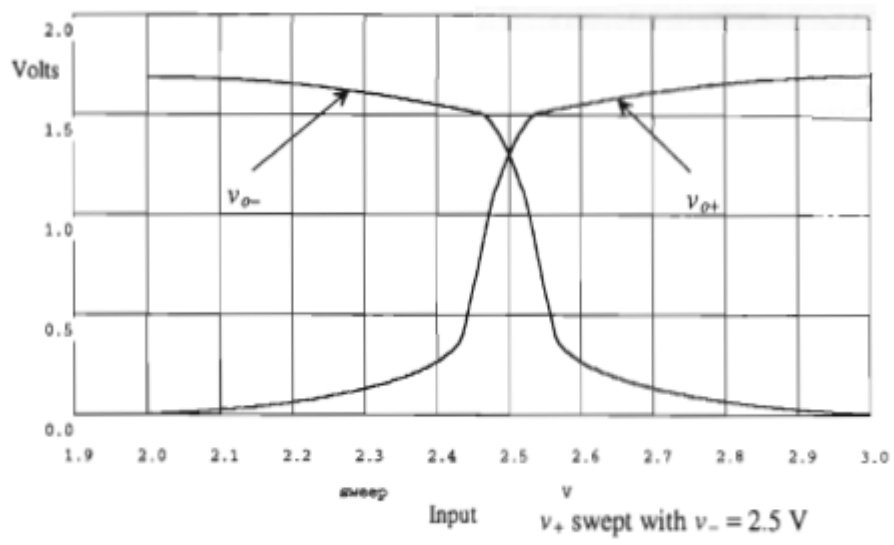


Fig3.5.b-simulative result

### 3.6 OUTPUT BUFFER:-

The last component of the comparator is an output buffer or postamplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal. The output buffer accepts a differential input signal and the essential requirement is not to have a slew rate limitation.

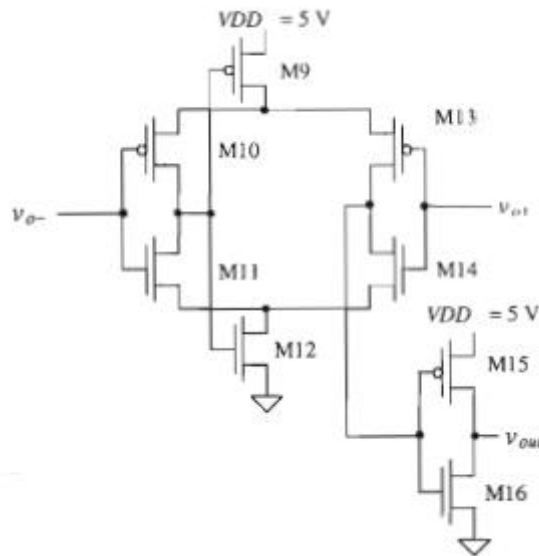


Fig 3.6.a-self biased differential amplifier

The circuit is a self-biased differential amplifier.

At the end an inverter is added on the output of the amplifier to provide additional gain and to isolate any capacitance from the differential amplifier.

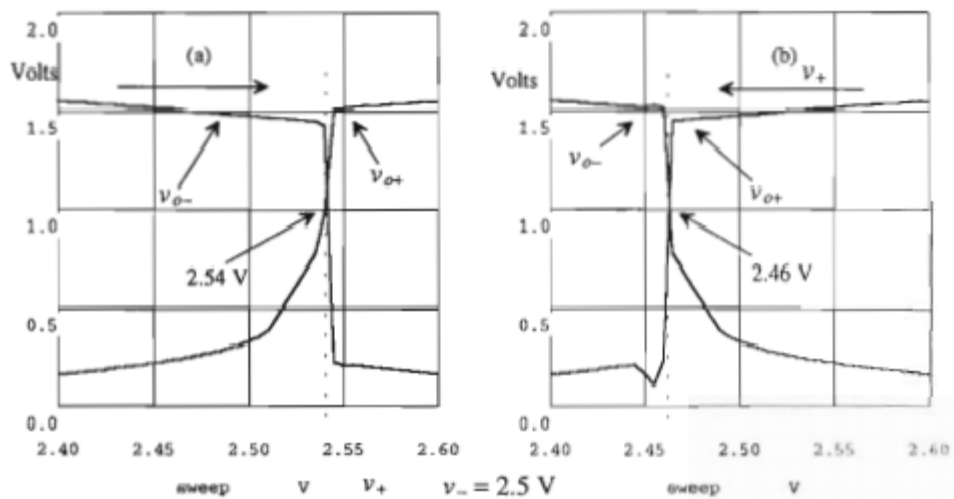


Fig 3.6.b-resolution of comparator

The resolution is calculated to be 40 mV.

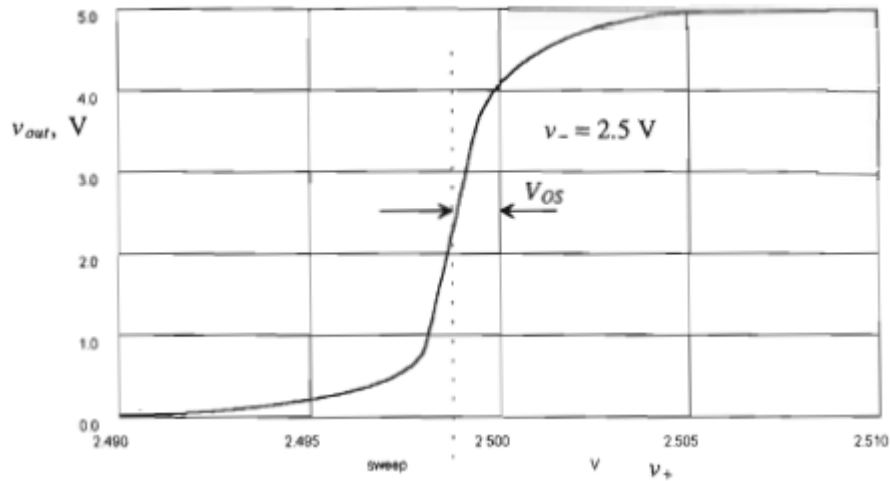


Fig 3.6.c DC characteristics and offset voltage

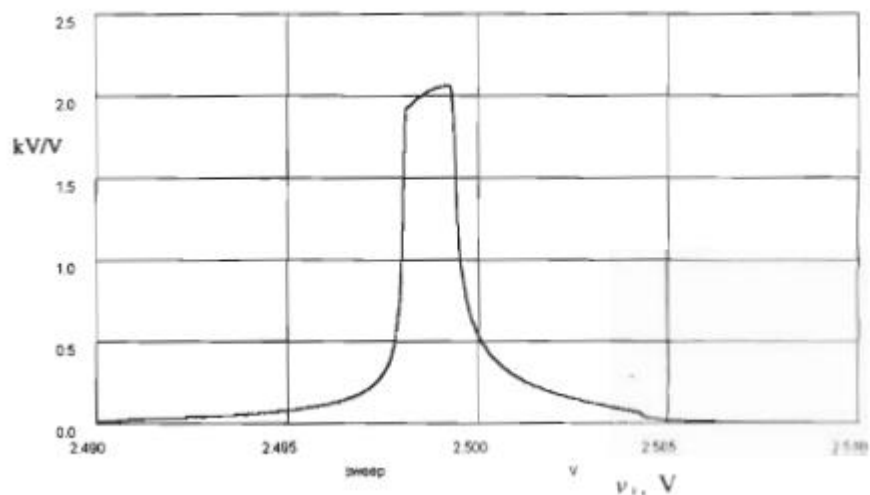


Fig 3.6.D. showing gain of comparator

The maximum the gain the resolution is less.

To increase gain  $g_m$  of M1 and M2 are increased

For further increase in gain M3 and M4 are resized w.r.t M31 and M32.

$V_{sph}$  and  $V_{spl}$  should be  $V_{dd}/2$  and  $V_{O+}$  and  $V_{O-}$  should cross each other at  $V_{dd}/2$  in order to have less offset. From transient analysis we can determine propagation delay.

## **CHAPTER 4:**

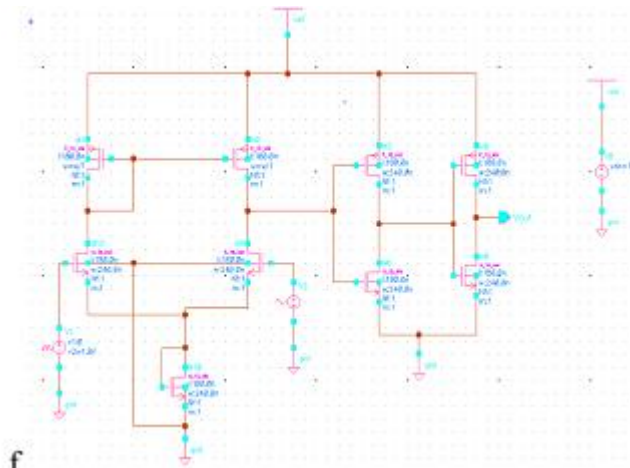
# **STRUCTURE AND OPERATION OF CIRCUITS**

## A.DESIGN 1

Design 1 is an open-loop comparator that consists of three stages and the circuit diagram is Shown in figure 1 .Advantage of this comparator is that a minimal number of MOS devices are used, and the circuit area is small. However, rather large currents will be needed to achieve the desired operation. Input section is a differential amplifier and output

Section is a push pull inverter. The input (first) stage has to amplify the minimal input signal and is shown in figure 4.1.

The high Trans conductance of this differential stage will provide large gain. Tran's conductance is increased by increasing the width of M1. The values of W1 and W2 are determined by the MOST (Saturation region) equation. However, this value will be adjusted depending on the simulation.





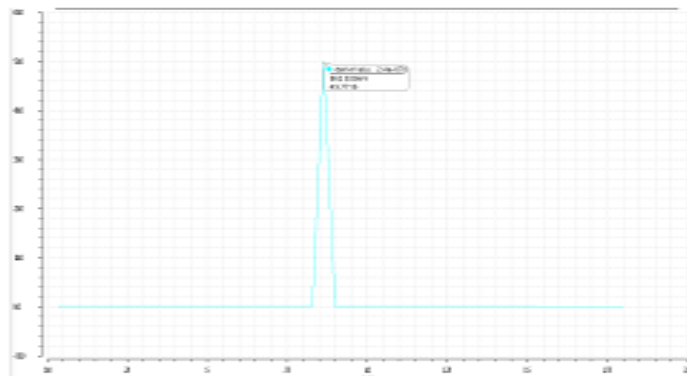
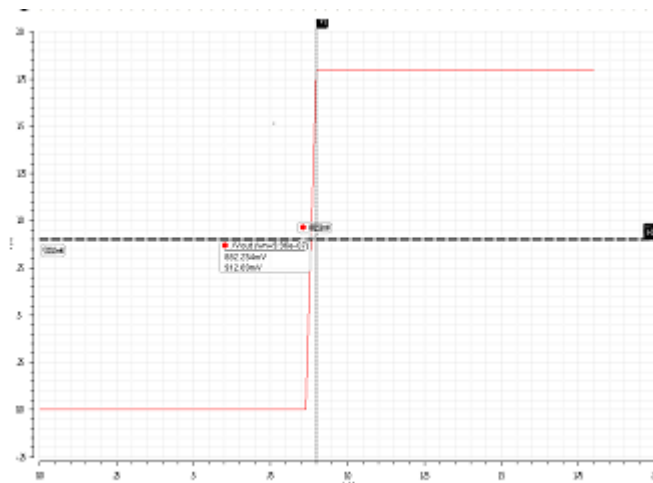


Fig 4.1.schematic, dc response, gain plot

## Simulation and results

Offset-40.032mV

Dc gain-38.6 v/v

Resolution-0.486 v

Power -412 uW

## 4.2 PREAMPLIFIER BASED COMPARATOR

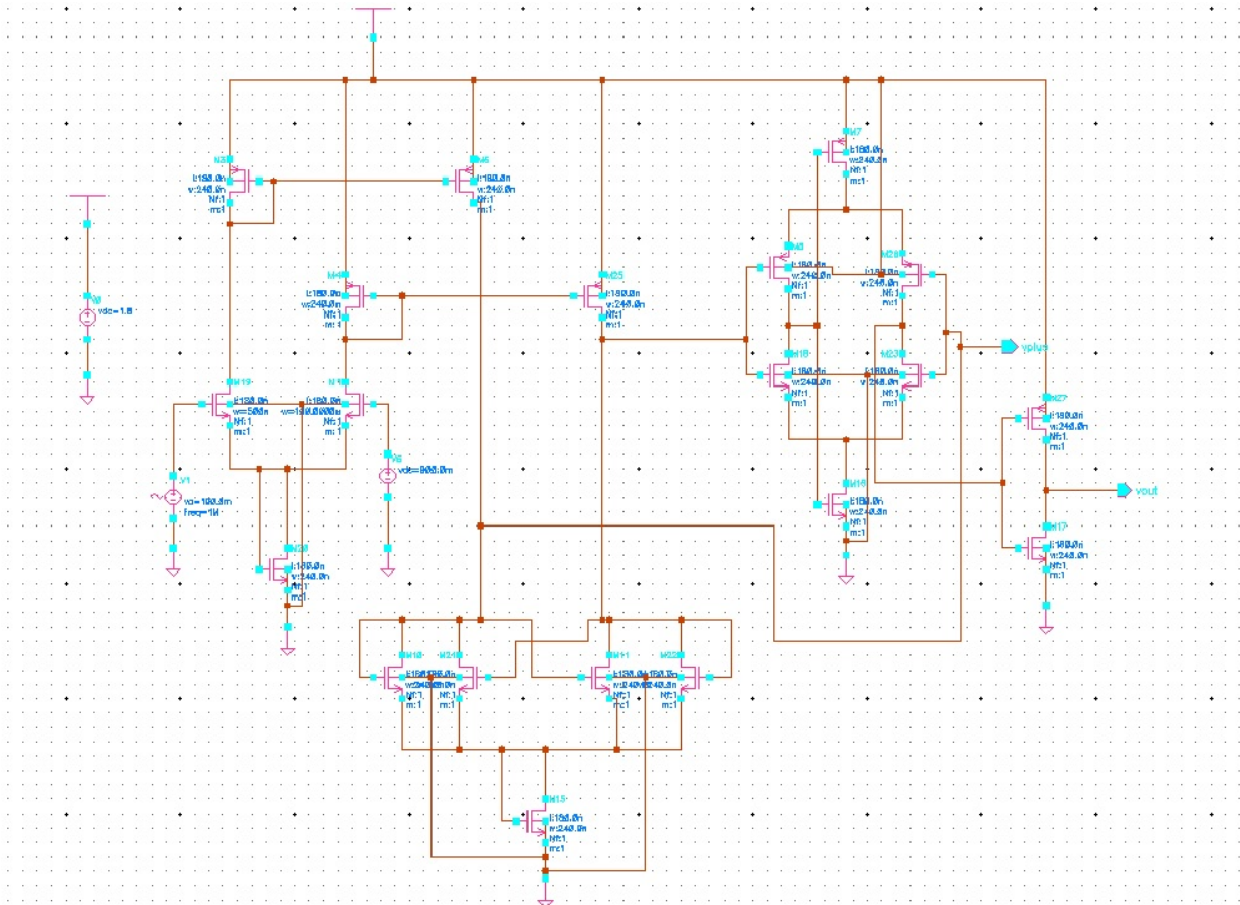


Fig 4.2 (i) schematic of preamplifier based comparator

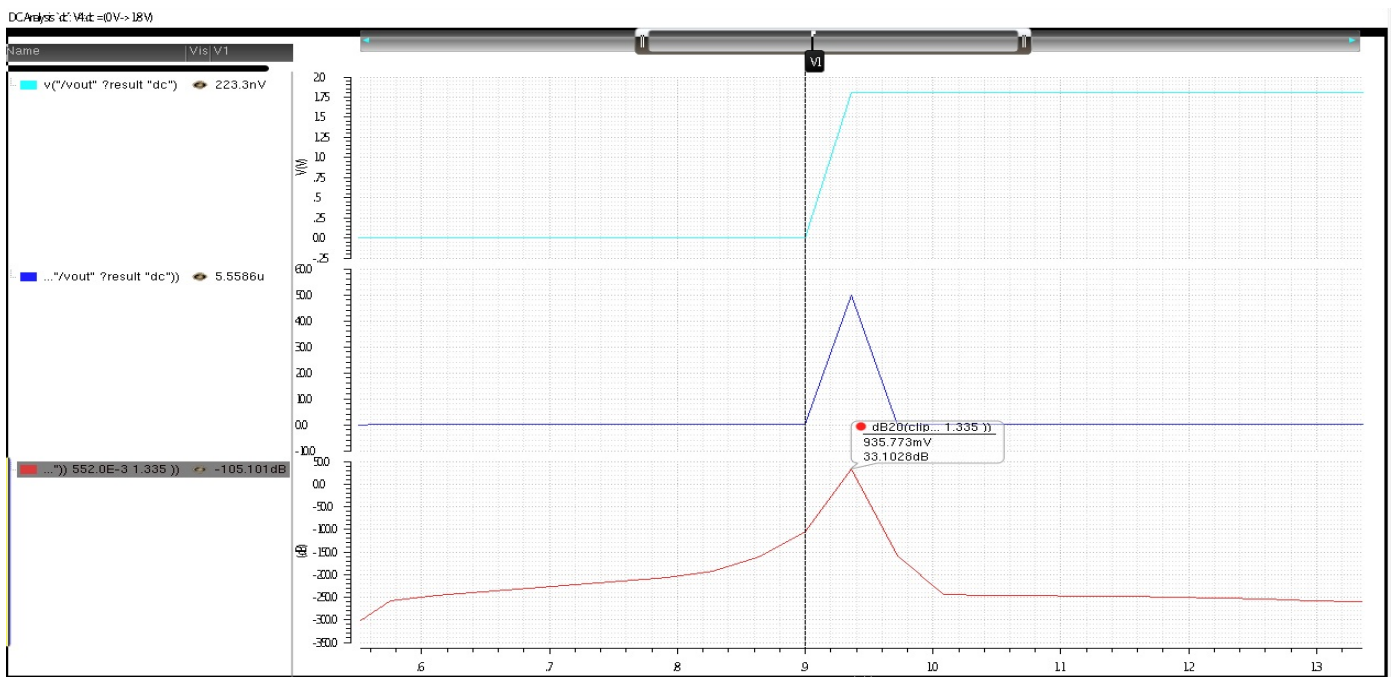
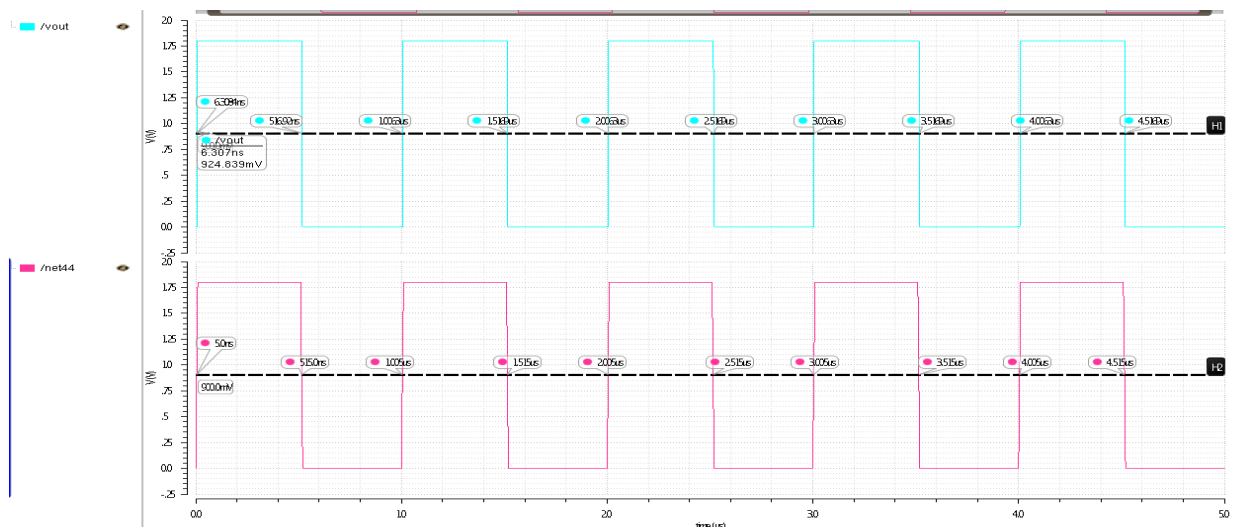


Fig 4.2(ii) dc response gain



#### 4.2.(iii)Simulation and results

Offset-45.032mV

Dc gain-42.6 v/v

Resolution-0.0194 v

Power -282 uW

4.3 Three stage preamplifier based comparator

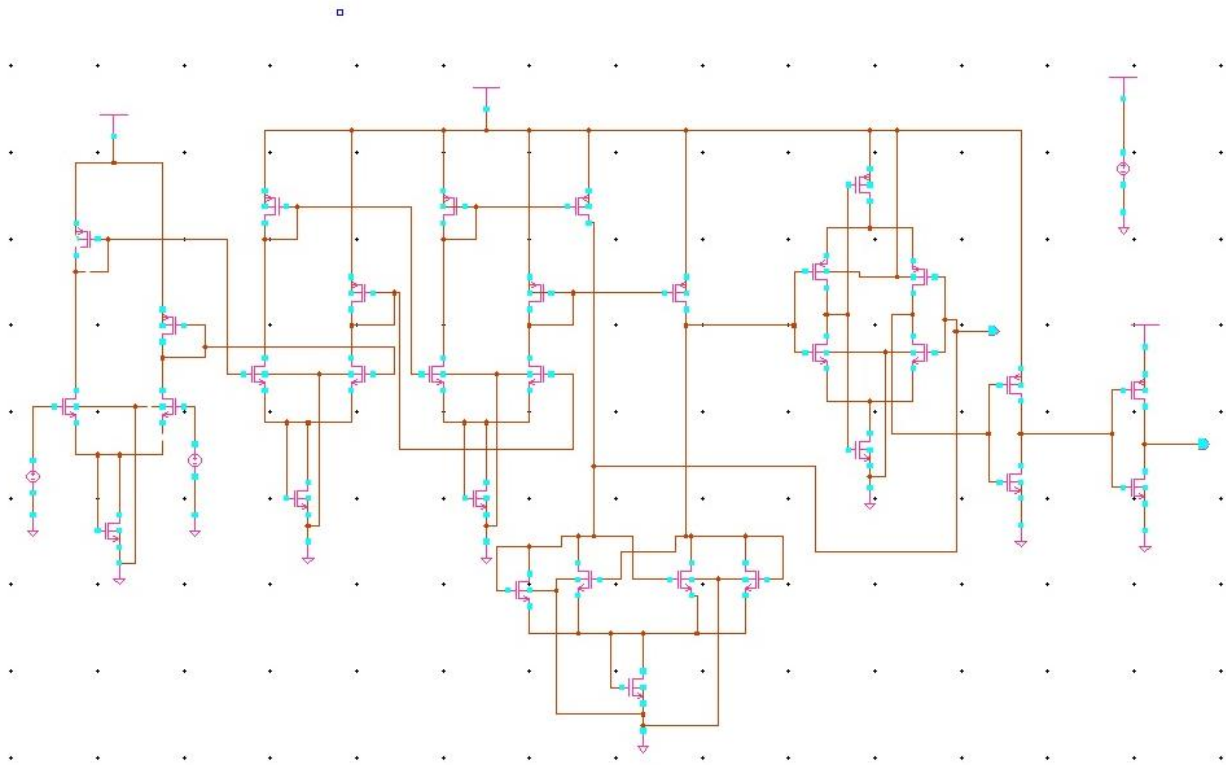


Fig 4.3(i) Schematic of three stage preamplifier based comparator

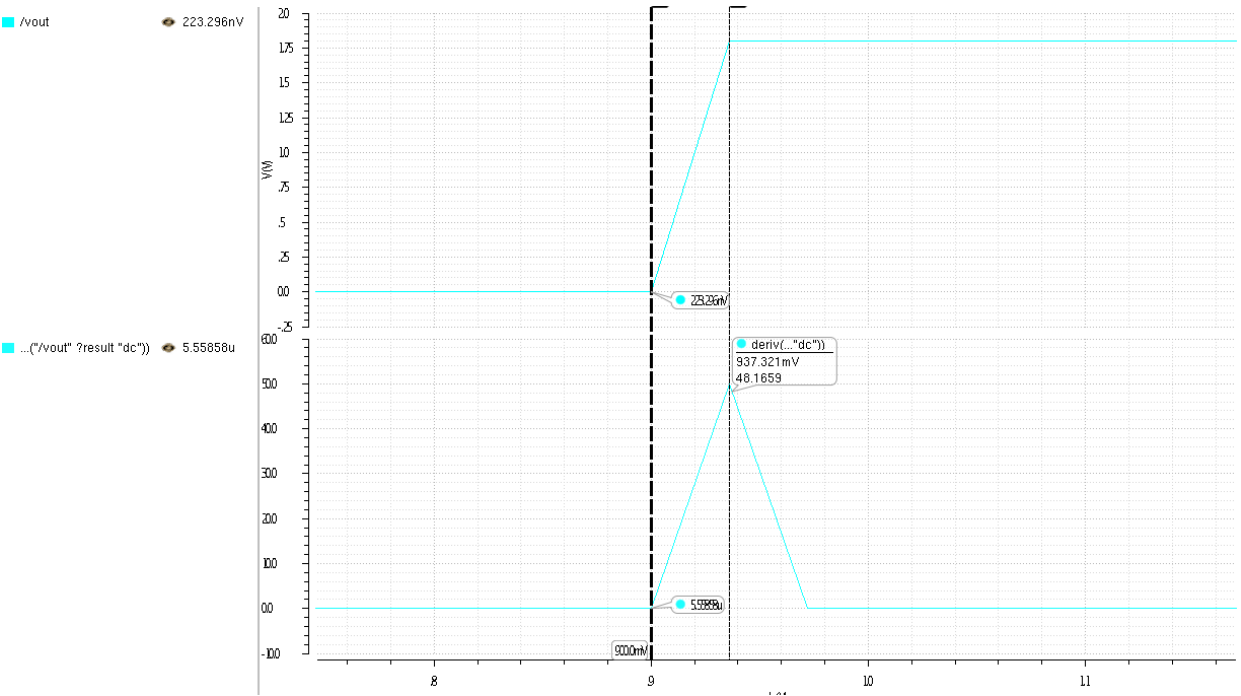


Fig 4.3(ii) DC analysis

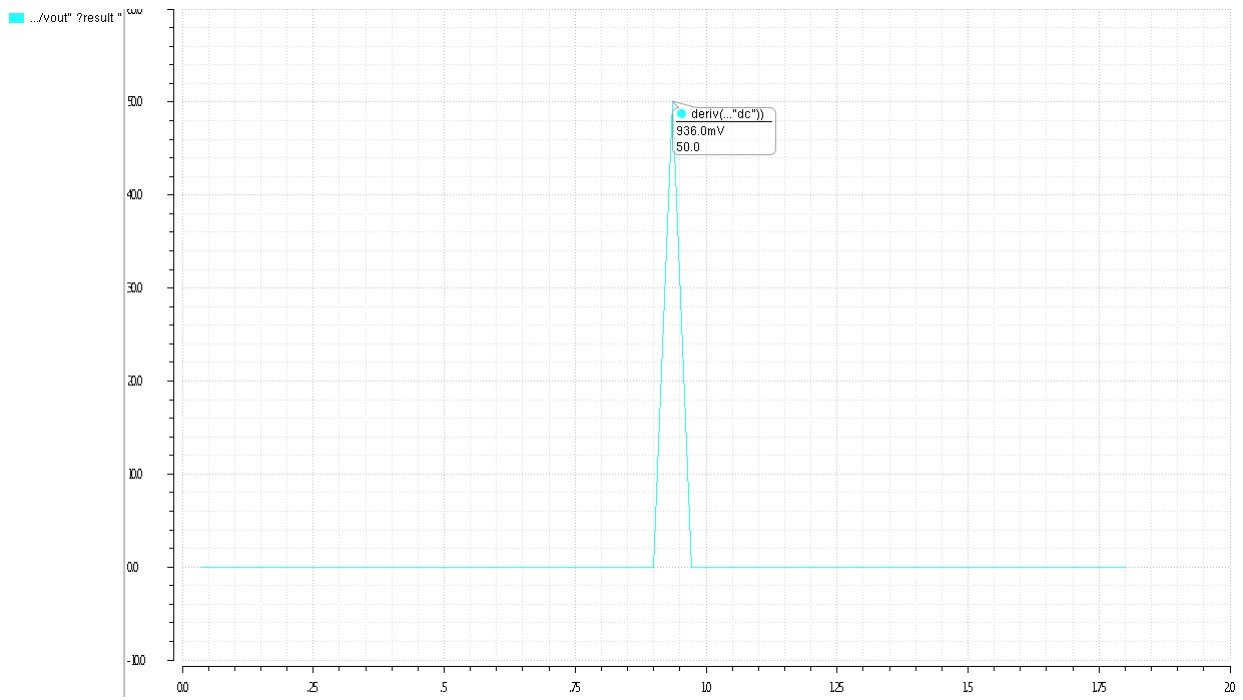


Fig 4.3 (iii) DC gain

## Simulation and results

Offset-40.032mV

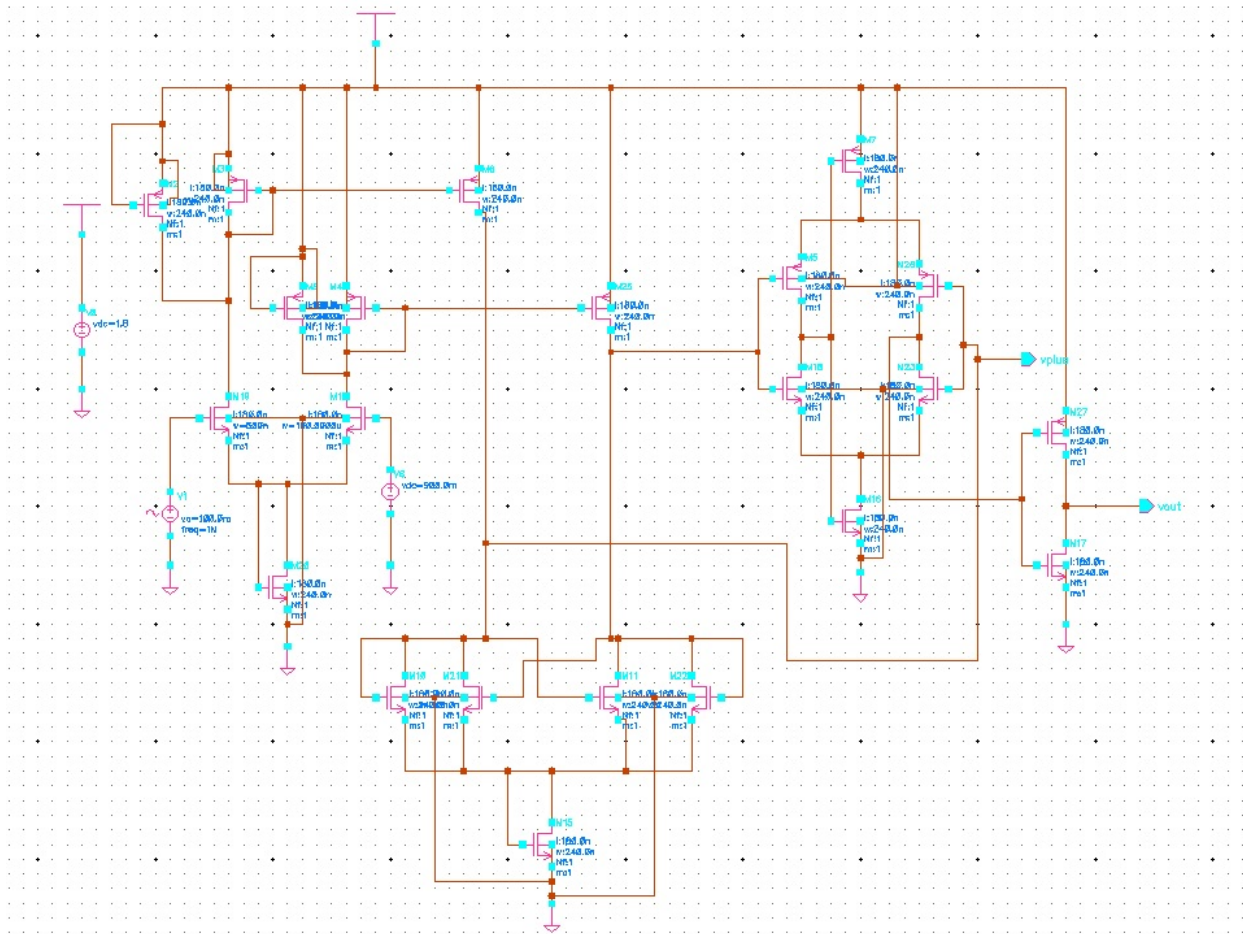
Dc gain-50.6 v/v

Resolution-26mV

Power -336 uw

#### 4.4. Modified preamplifier

Differential amplifier using p-mos. transistor and a p-mos. current source as load



4.4. (Fig i) Schematic of modified preamplifier based comparator

Circuit operation: - we can increase gain by reducing gm3. This can be done by reducing the current through M3, so we connect a current source in parallel.

$$A_v = \frac{g_{m3}}{g_{m1}} = \frac{K_n \left(\frac{W}{L}\right)_1}{K_p \left(\frac{W}{L}\right)_3} \sqrt{1 + \frac{I_5}{I_3}}$$

If  $I_5 = 24(I_3)$

The gain will increase by 5 times

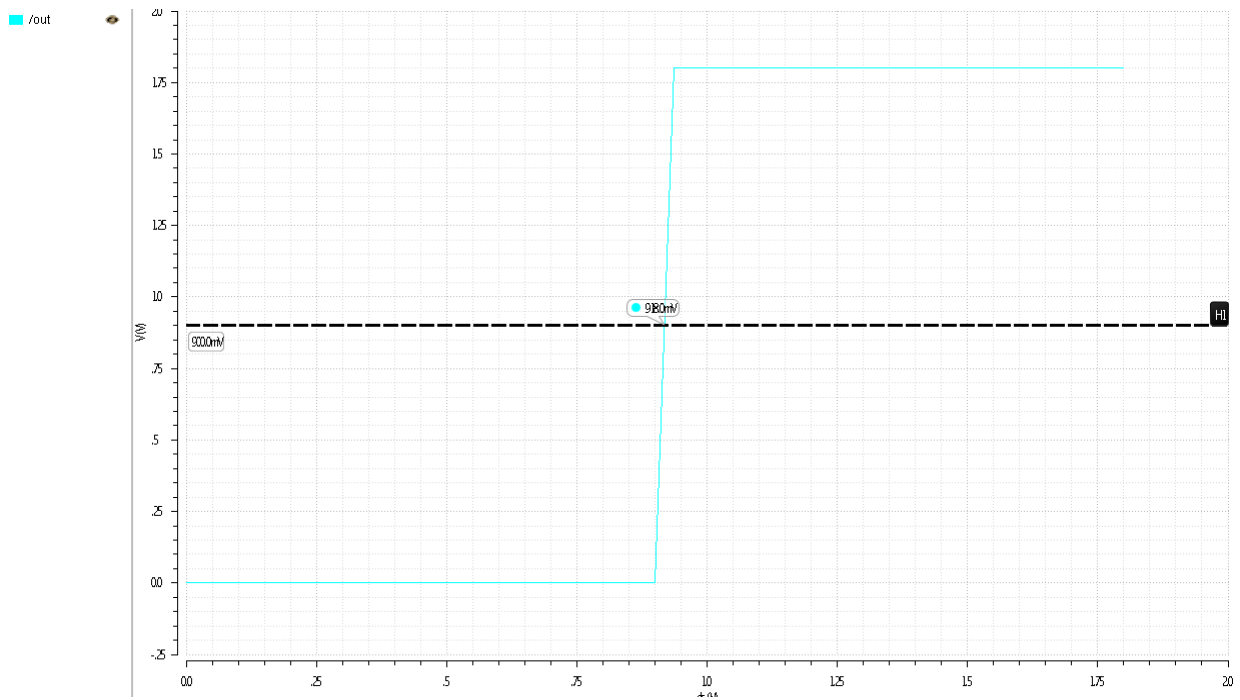


Fig 4.4.(ii)DC response of modified preamplifier based comparator

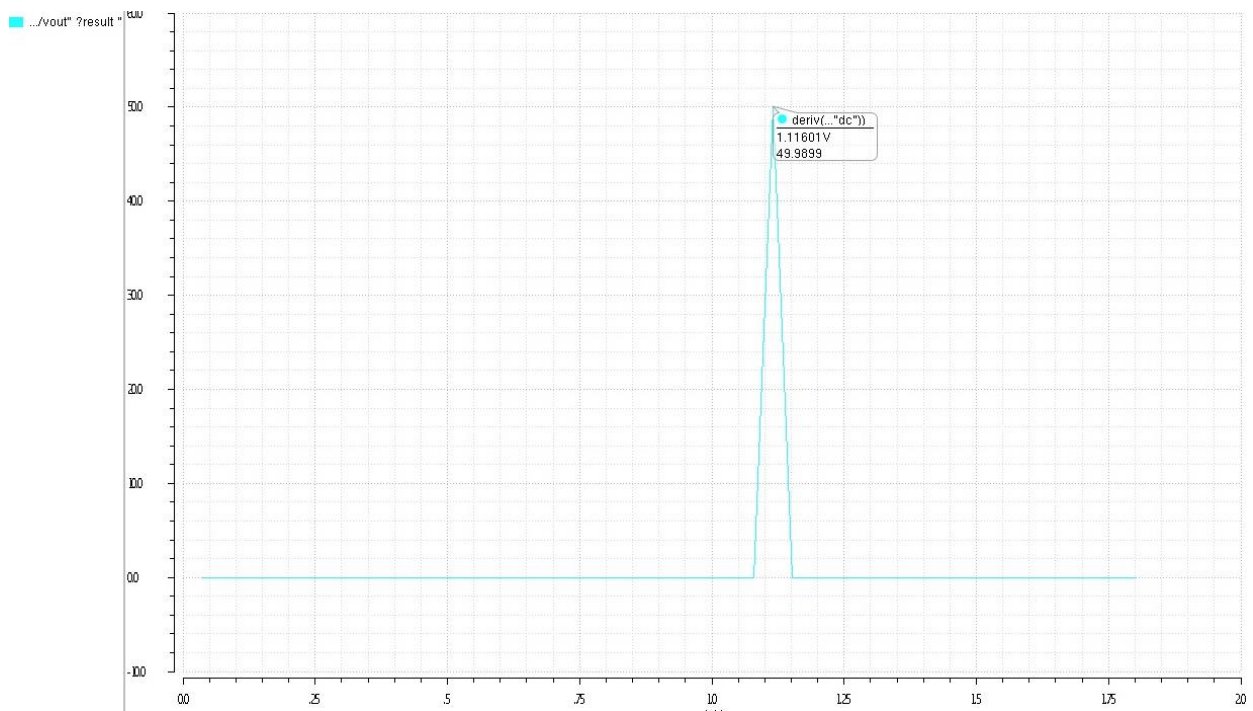


Fig 4.4.(iii) DC gain of modified preamplifier based comparator



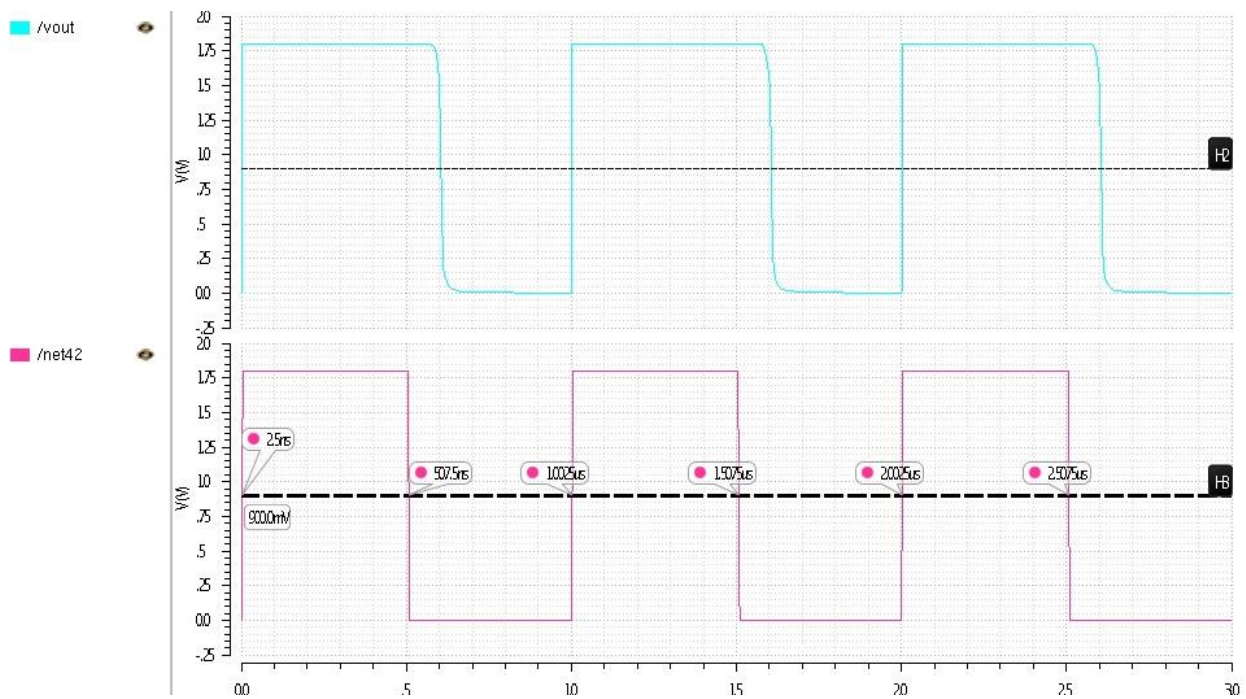


Fig 4.4(iv) Transient analysis

Simulation and results

Offset-40.032mV

Dc gain-49.99 v/v

Resolution-0.0360m v

Power -237uw

Propagation delay=1.247ns



## 4.5: Negative resistance in parallel as load

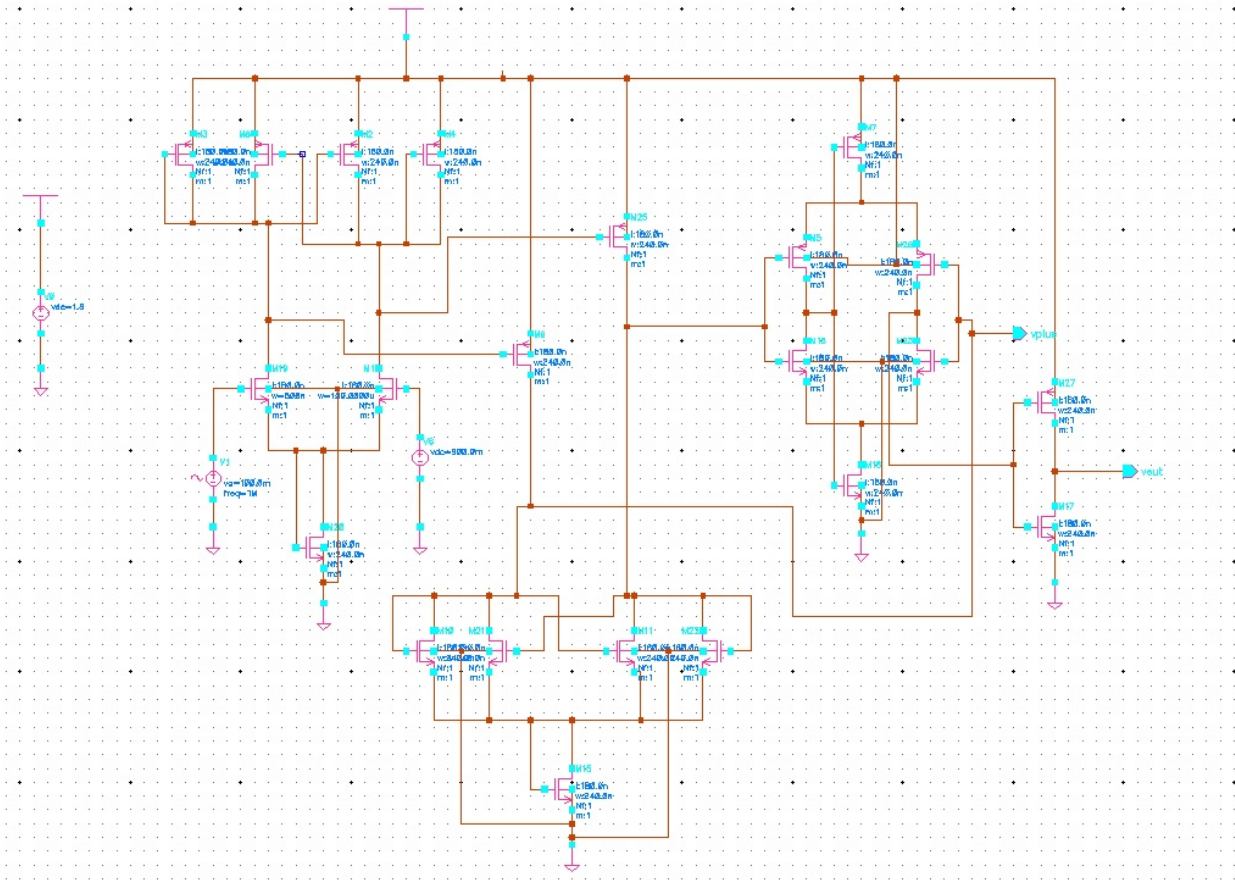


Fig 4.5(i) Schematic of negative resistance in parallel as load

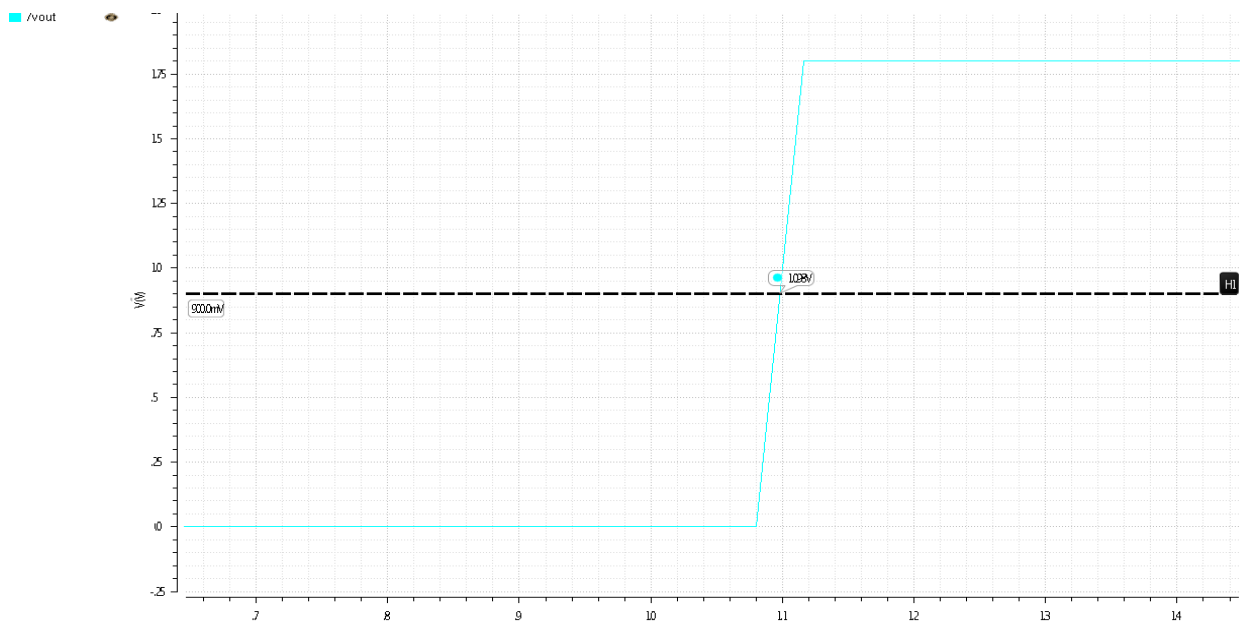


Fig 4.5(ii) DC response of negative resistance in parallel as load

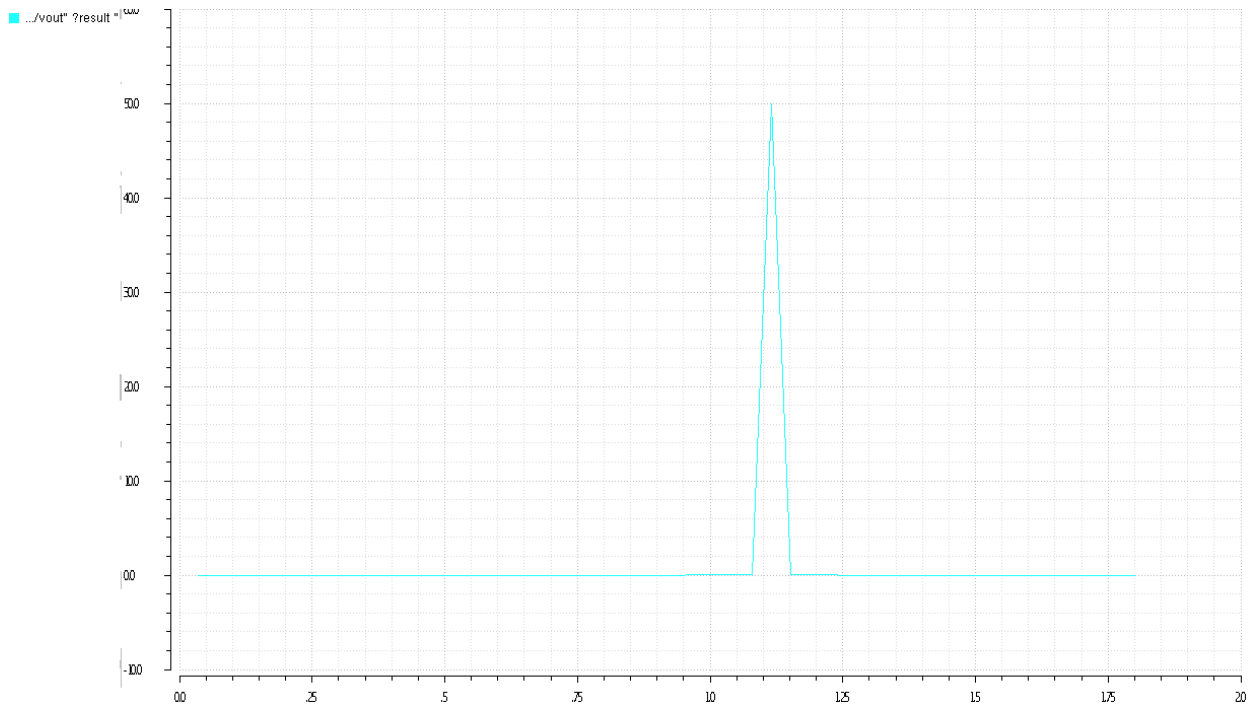


Fig 4.5(iii) DC gain of negative resistance in parallel as load

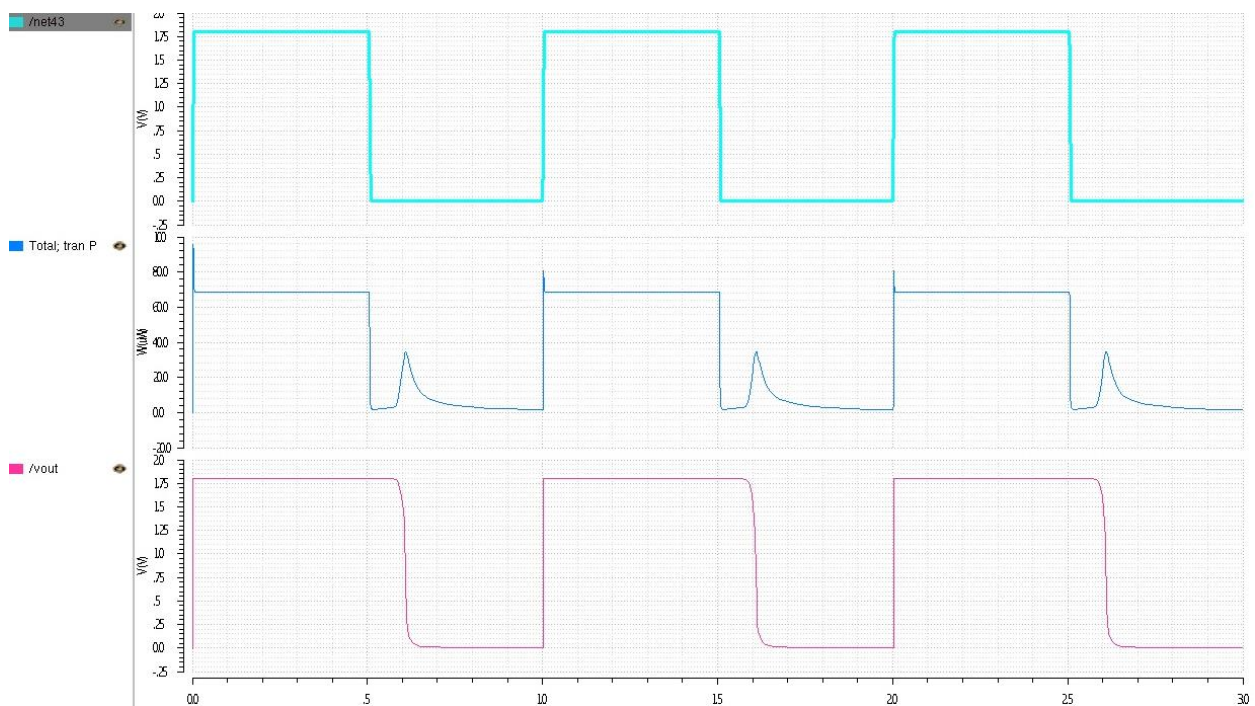


Fig 4.5(iv) Transient response and power plot

Propagation delay=1.56ns

#### 4.6: Comparator with excitory feedback

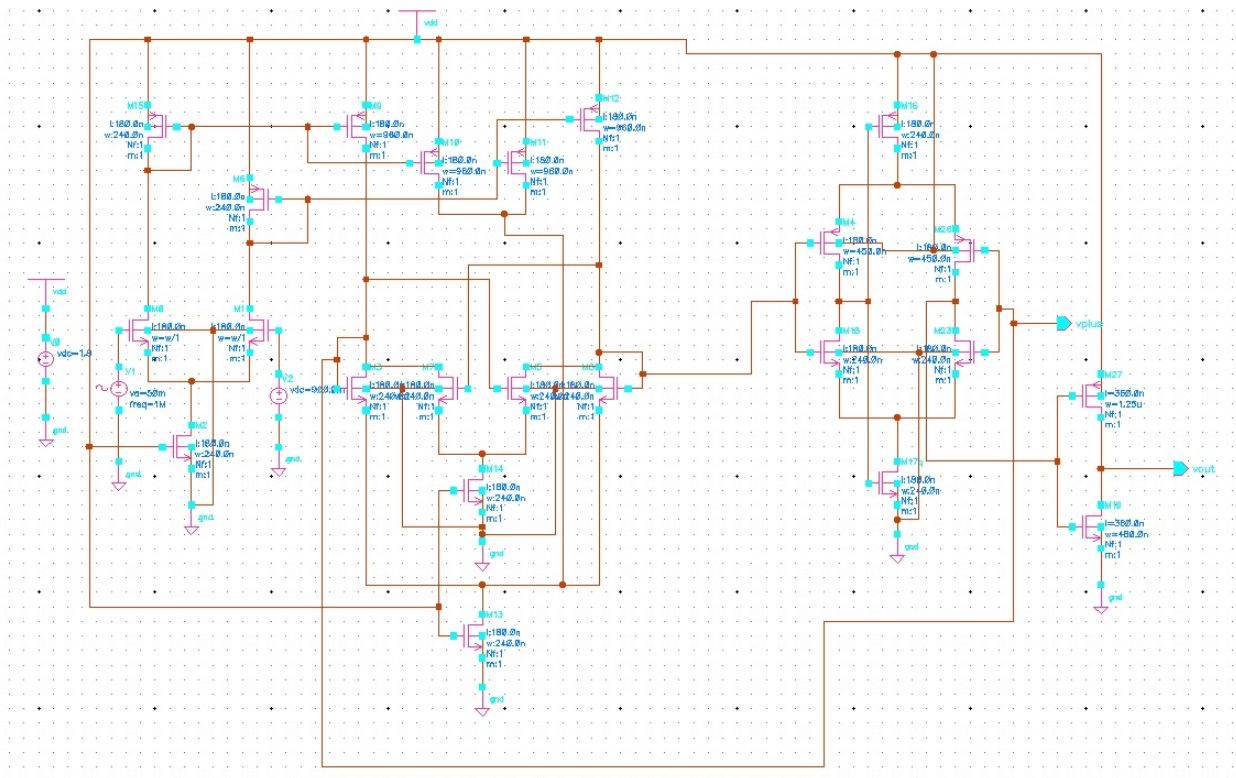


Fig 4.6.(i) Schematic of comparator with excitory feedback.

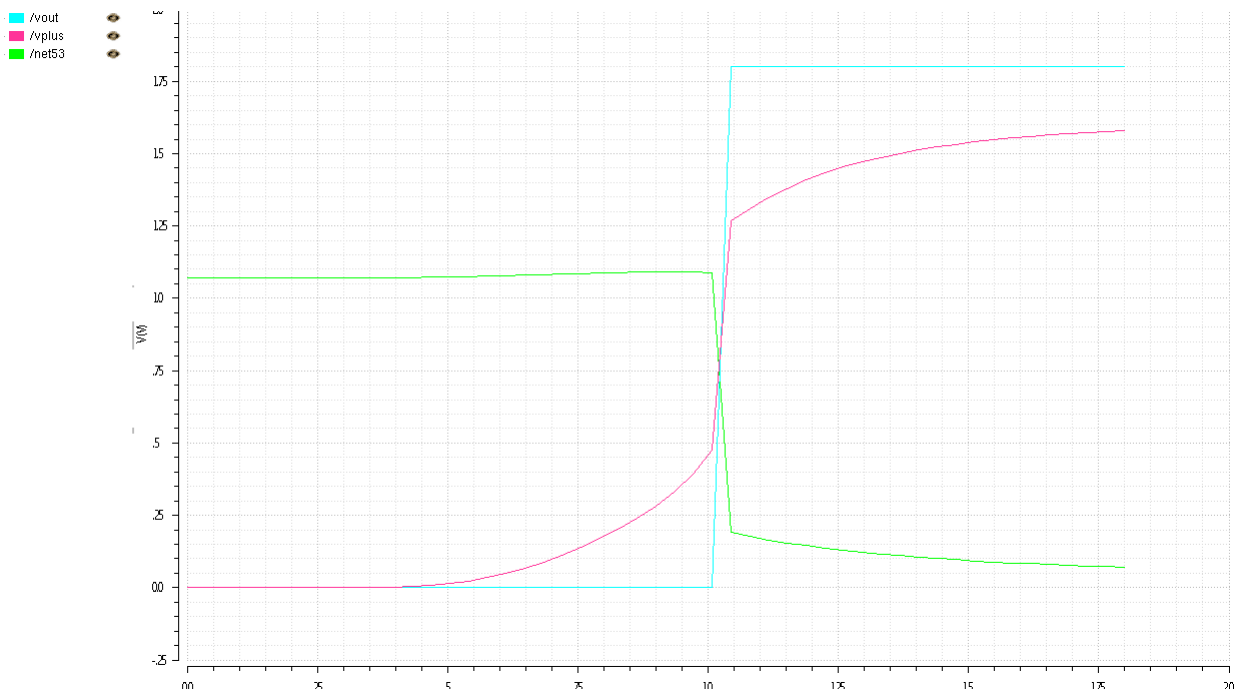


Fig 4.6.(ii)DC response of comparator with excitory feedback.

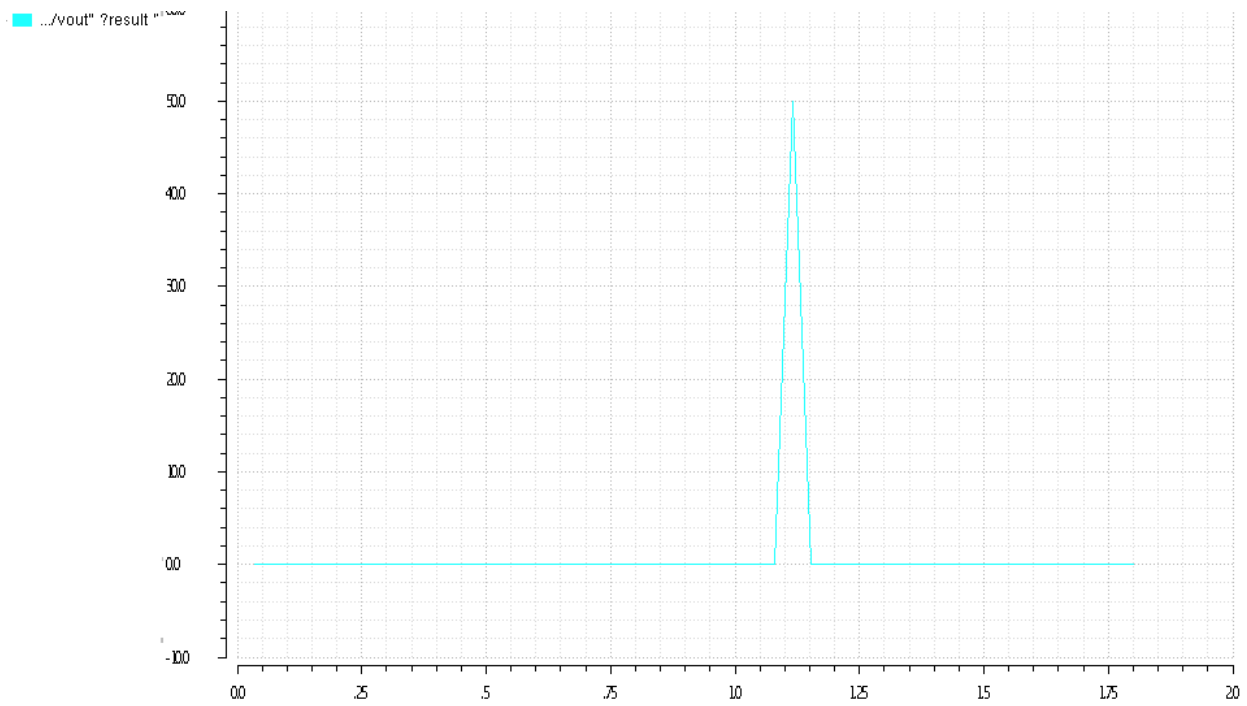


Fig 4.6.(iii) DC gain of comparator with excitory feedback.

## Simulation and results

Offset-0.036mV

Dc gain-50 v/v

Resolution-0.486 v

Power -412 uw

Propagation delay=0.352ns

## **CHAPTER 5**

# **DESIGN PRINCIPLES FOR LOW POWER VLSI**

## 5.1 Introduction

During the earlier invention of the transistor, the Designers gave emphasis to optimize area, high performance, reliability and low cost. The secondary consideration was “Power”. Now the trend has started to change, power is being given equal importance to area and speed.

The emerging trend in electronic industry is low power design. The importance of low power has caused a designing modification where power dissipation has become as important consideration as well as performance and area. This chapter gives various techniques and methodologies for the designing of low power circuits and systems. The main focus of the chapter is the issues faced by the designers at various level of design i.e architectural, logical, circuit and device levels. Some of the techniques are proposed to overcome these difficulties.

In fact, battery-powered applications drove low power electronics –such as pocket calculator, hearing aids, implantable pacemaker, portable military equipment used by individual soldiers and most importantly wristwatches. For all such application, longer the battery could last, the better. Consequently, ever since then, power requirement reduction has become one of the most critical factors in the evolution of microelectronics technology.

## 5.2. Power Dissipation sources:

There are 3 sources of power dissipation in digital CMOS circuits.

- A. signal transition
- B .short circuit current
- C. leakage current

### A. signal transition:

Due to the transition of supply voltage between two state between VDD and ground the capacitances associated with the node gate charged and gets discharged. Due to this effect Current flows through the channel and heat is dissipated away. This power is proportional to the applied voltage.

### B .short circuit current:

Another source of power dissipation arises from the short circuit current, that flows directly from the VDD to the ground terminal. This is due to conduction of n and p sub network simultaneously.

### C. leakage current:

The last source of power dissipation is due to the leakage current that flows when input and the outputs of a gate are not changing. And it's called static dissipation as shown in figure below.



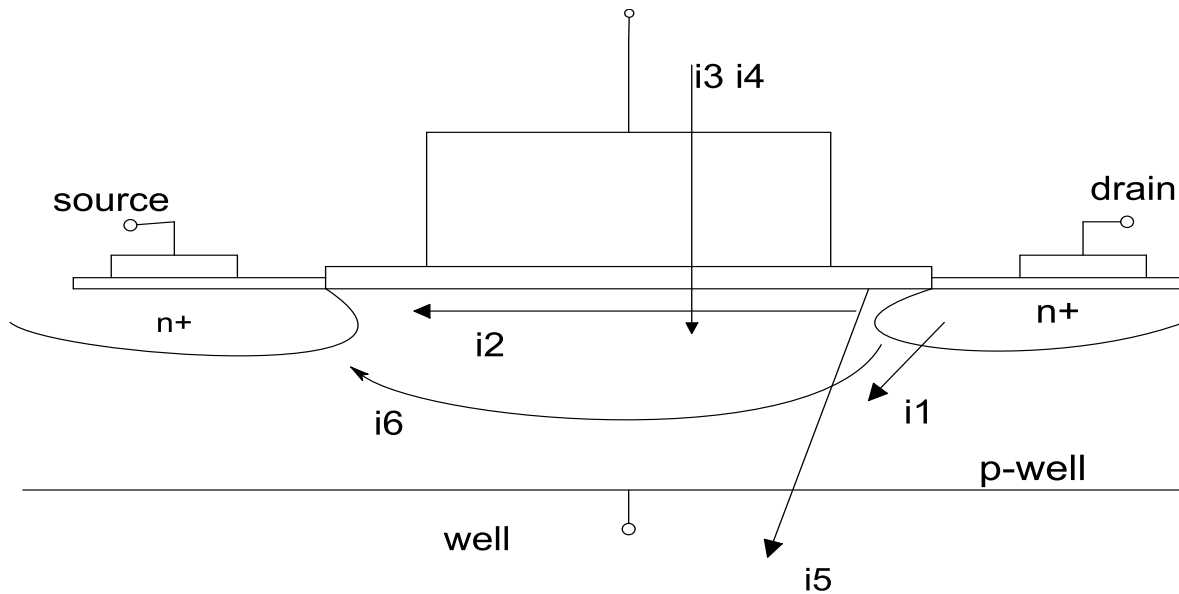


fig 5.1 leakage current in MOSFET

- i1= Reverse bias pn junction current
- i2= The leakage current due to sub threshold operation
- i3= Gate oxide current due to tunneling.
- i4= hot carrier injection current.
- i5= GIDL current
- i6= punch through current

Active power dissipation:

$$\text{Short circuit power} = p_{sc} = \frac{\beta}{12} (V_{DD} - V_{TH})^3 \frac{\tau}{T}$$

It depends upon frequency, supply voltage, rise and fall time of input signal.

Switching dissipation:

It depends upon switching frequency and square of the supply voltage.

# **CHAPTER 6:**

## **DESIGN OF DYNAMIC COMPARATOR**

## 6.1. INTRODUCTION

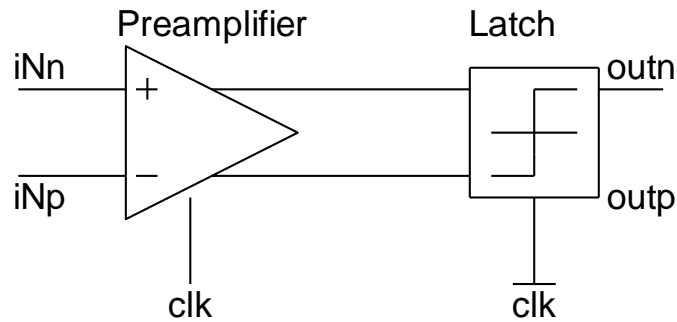


Fig 6.1 clocked comparator

Clocked comparator is often called dynamic comparator. Some comparators are clocked and after the transition of the clock. The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition. The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low. Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators. Dynamic comparators are widely used in the design of high-speed ADCs.

## 6.2: Preamplifiers

Low gain ( $4 \sim 10$ ) for high speed, used for higher resolution and reduction of kickback effects. Kickback denotes the charge transfer either into or out of the inputs when the TAL stage goes from track mode to latch mode. Without a preamplifier, it causes very large glitches in the input circuit, especially when the input impedances are not perfectly matched  $\rightarrow$  limited accuracy.

The track-and-latch stage: amplifies the signal further during the track phase, and then amplifies it again during the latch phase by positive feedback  $\rightarrow$  minimizes the total number of gain stages. Hysteresis might be eliminated by connecting internal nodes to one of power supplies or by connecting differential nodes together (no memory). For high resolution, coupling capacitors and reset switches are included to eliminate any VOS errors.

### 6.3: LATCH

A latch is a regenerative type of comparator that uses positive feedback to accomplish the comparison of two signals. The simple form of a latch is shown *figure 3.9* and consists of inverters in positive feedback. Suppose that nodes  $V_x$  and  $V_y$  have an initial voltage level and by opening the switch, the circuit is placed in the regenerative mode. At this instance the feedback

is enabled and the outputs will change in a certain time period ( $V_x = \text{low}$  and  $V_y = \text{high}$ , or visa-versa). This time constant of the latch can be found by analysing a simplified circuit as shown in *figure 3.9*. With the assumption that the inverters are in their linear range, the inverters can be modelled as voltage controlled current sources, driving an RC load.  $A_v$  is the low frequency gain of inverter and for this linearized model *equation 3.10* holds.

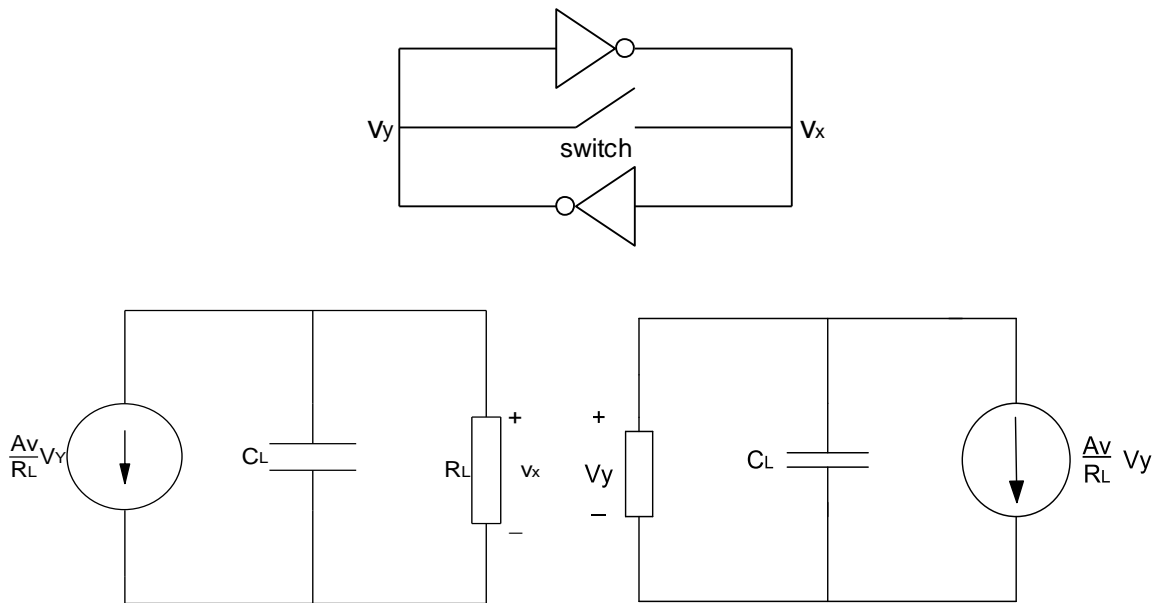


Fig 6.3(i) : Simplified latch circuit

Multiplying *equation 3.10* gives,

$$\tau \left( \frac{dV_x}{dt} \right) + V_x = -A_v V_y$$

and

$$\tau \left( \frac{dV_y}{dt} \right) + V_y = -A_v V_x$$

where  $T = RLCL$  is the time constant at the output node of each inverter. Subtracting the last two equations, *equation 3.13* is obtained.

$$\left(\frac{\tau}{A_V - 1}\right)\left(\frac{d\Delta v}{dt}\right) = \Delta v$$

Where  $t:: V = V_X - \sim$  is the voltage difference between the output nodes of the two inverters.

The solution for this first-order differential equation is given by,

$$\Delta V(t) = \Delta V_i \cdot e^{(A_V - 1)t/\tau}$$

b.  $V_i$  is the initial voltage difference at the beginning of the latch phase. Thus, the voltage difference increases exponentially in time, with a time constant given by *equation*

$$\tau_L = \frac{\tau}{A_V} = \frac{R_L \cdot C_L}{A_V} = \frac{C_L}{G_M}$$

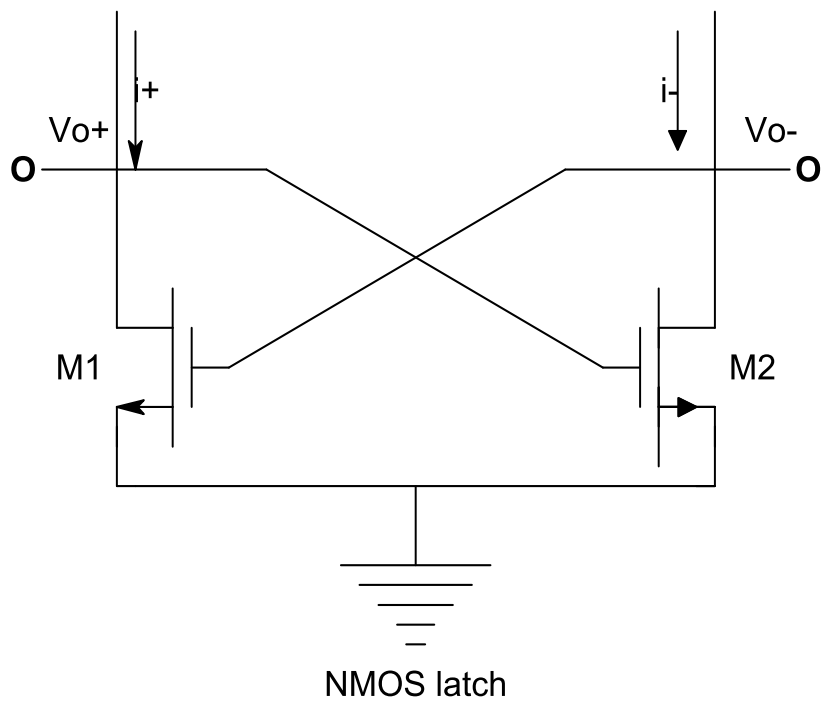
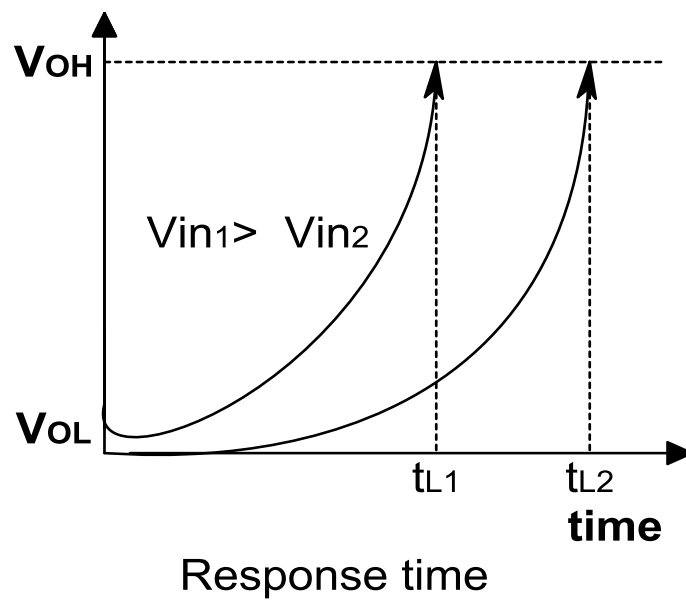
$G_m$  is the trans conductance of each inverter.  $CL$  is the capacitance seen from each inverter. The propagation time delay of the latch can be found from the previous equations, by setting the output level to  $V_{oL}$ . Thus the propagation time delay is given by

$$t_p = \tau_{L=l_n} \frac{v_{oH} - v_{oL}}{2 \cdot \Delta v_i}$$

The time required for the output to reach maximal output level is decreased by applying a larger input difference to the latch ( $b.V_i$ ). If the input is small, the latch takes a long time to reach the maximal output level, *as shown in figure 3.10(a)*. Therefore, it is desirable to apply a larger input signal in order to take advantage of faster latch response. If the input signal is low, the

Preamplifier circuit can be used to achieve shorter response time. A major advantage is that the power dissipation of the latch is relatively small compared to the differential amplifying circuit.

Latch only dissipates the dynamic power. In below *the* latch circuit is shown, where the n-channel MOST is used.



Latch response time and n-channel MOST latch circuit

## 6.4: Comparator offset

Due to the mismatch between input transistors, the circuit exhibits a dc offset of different values. This value of dc offset depends on the mismatch of input and output voltages. The figure 6.4(i) shows a differential pair with perfect symmetry of input and output nodes, i.e.  $V_{in} = 0$  as well as  $V_{out} = 0$ , hence the circuit has no offset error. On the other hand if the input is zero and output is not equal to zero, the circuit exhibits mismatch and suffers a dc offset. This dc offset is equal to the value of  $V_{out}$  when the input voltage ( $V_{in}$ ) is zero, and is called the output referred offset. The input-referred offset voltage can be defined as the input level which forces the output voltage to go to zero [6]. The offset can limit the performance of comparator and can make the system nonlinear. The precision 10 of the comparator is also affected by the offset.

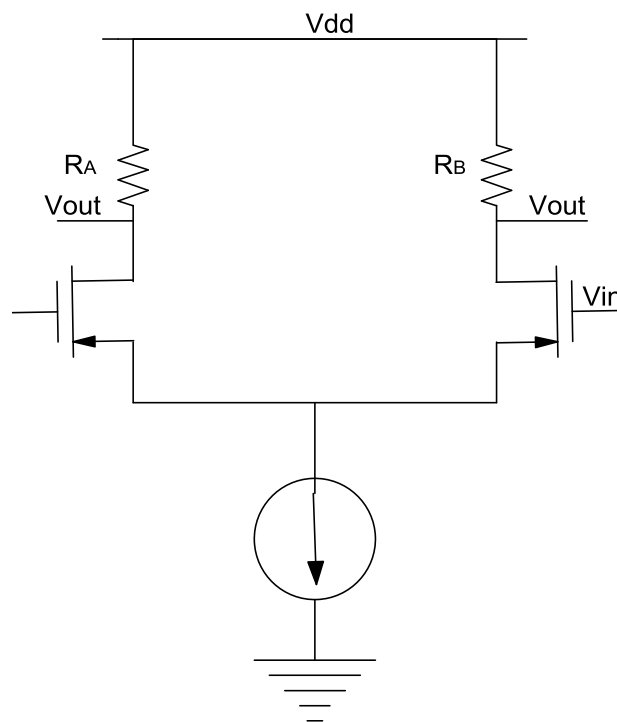


Fig 6.4(i) Differential pair with offset measured at the output

#### 6.4. a: Kickback

During the regeneration process the latched comparator uses the positive Feedback mechanism to scale the digital level. The voltage variations at the Regeneration nodes are coupled to the inputs and disturb the input voltages. This disturbance is called the *kickback* noise. There are many solutions to this problem, a few techniques are discussed in later chapter.

#### 6.4. b: Sampling switches

A sampling circuit consists of a capacitor and switch (a MOS transistor) Controlled by the clock. The sampling switch is placed before the comparator Inputs. During the regeneration phase these switches are opened and Disconnect the inputs from rest of the circuit [7]. The switches should be sized as small as possible compared to the total capacitances at the inputs to minimize the effect of charge injection .

#### 6.4. c: Isolation transistors

Isolation transistors isolate the input differential pair from the regeneration process. Isolation transistors are usually a set of NMOS transistors controlled by the clock and placed between the drain of differential pair and regeneration outputs. During the regeneration phase the isolation transistors are switched off preventing the charge injection to the differential inputs. This technique results in low kickback noise.

#### 6.4.d: Pre-amplifier

The pre-amplifier is the most commonly used solution placed in front of the comparator to reduce the kickback effect. The pre-amplifier also amplifies the input difference and reduce the input-referred offset[2]. The pre-amplifier may increase the gain and bandwidth of the system but power consumption is also increased.

#### 6.4.e: Neutralization technique

This technique is used in the designs where differential inputs are directly Connected to the regeneration nodes. Due to the non-zero impedance of the Circuit preceding the comparator, the inputs of the comparator are disturbed by the drain voltage variations of the differential pair. By adding the two capacitances between the gate and drain of the differential pair, as shown in figure , with a value equal to the  $C_{gd}$  of the



differential pair will cancel the kickback noise . This technique is further discussed in detail in later chapter.

#### 6.4.f: Parasitic

The parasitic play a critical role in analog designs. The ac behaviour of the MOSFET is crucially affected of parasitic. The figure 2.2 shows a simple model to illustrate the parasitic of a MOSFET. Between every two of four nodes of MOSFET, there exists a capacitance. The capacitance depends upon the gate voltage and it changes values according to the region of operations. The capacitances are; overlap capacitance between gate and source/drain, depletion capacitance between channel and substrate, oxide capacitance between gate and channel and junction capacitance between source/drain and substrate.

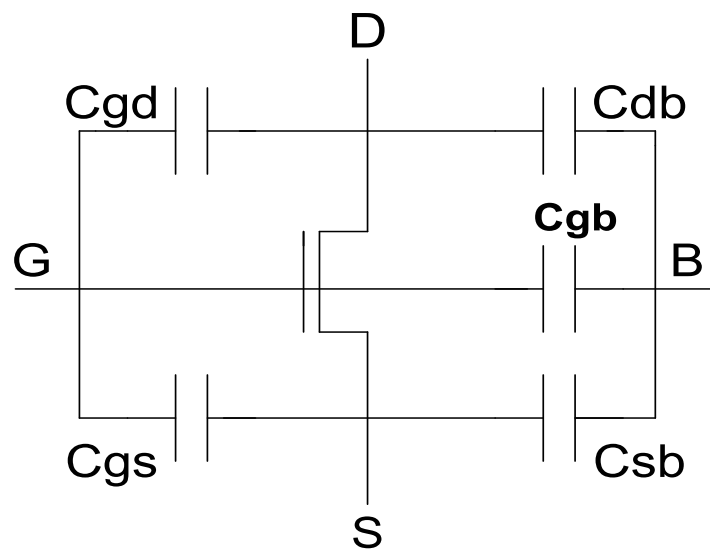


fig 6.4.II: MOSFET parasitic capacitance

## 6.4 .g: Meta stability

Normally in all latching comparators meta stability is a problem which occurs when the input is near the comparator decision point [9].

Comparator meta stability occurs when very small signals appear at the input of a comparator close to the comparator decision point. Normally all kind of latching comparators exhibit this problem [9]. In such cases, the comparator is not able to make a decision, i.e latch its output to the stable point, within the allotted time. This metastability delay is random and could switch the output to the wrong logical levels which can cause system malfunction or failure. The figure 2.3 shows the voltage transfer characteristics of two back to-back connected inverters. Each inverter has two stable points;  $V_{dd}$  or Ground. The mid-point where the two curves intercept each other is metastable point (MSP) as shown in the figure 2.3. Ideally the MSP of an inverter is at half of the input range i.e.  $V_{dd}/2$ . Now, if the input at the first inverter slightly deviates from  $V_{dd}/2$ , the output at the second inverter goes to one of the stable states. In this band of range the output is unpredictable and can switch to wrong logic level.

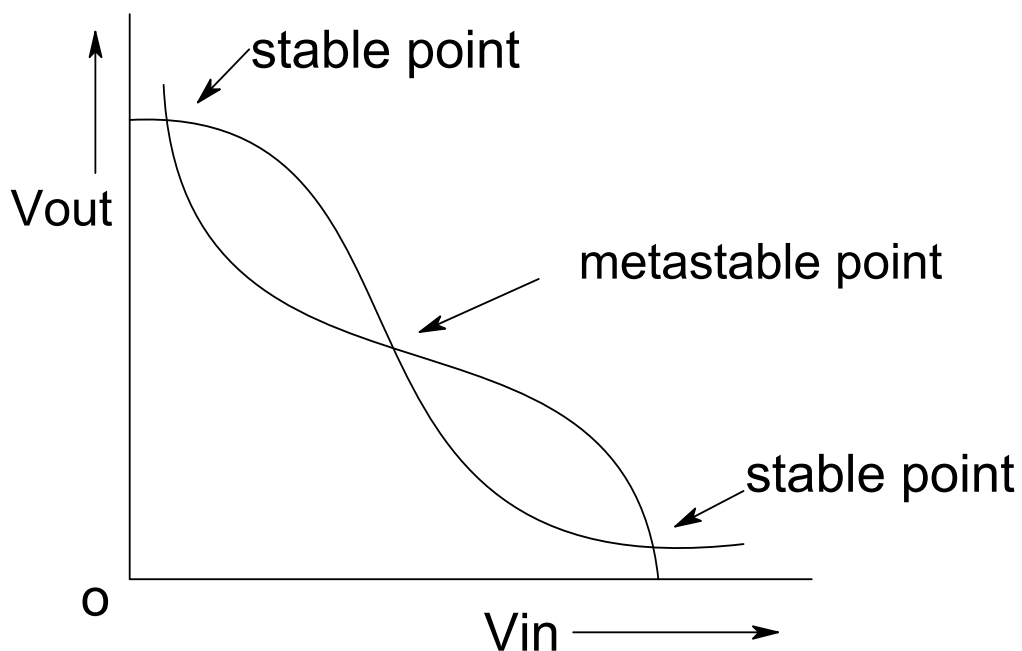


Fig 6.4. III .VTC of back-to-back connected two inverters.

## 6.5: Comparator types

Several comparator types are existing and depending on the design requirement, one topology will provide better results than the other. However, technology is a major boundary, and often the trade-offs must be made between the speed, resolution and the power dissipation. Topologies are divided into *Open-loop*, *Regenerative* or the combination of these two. In the case that the comparator is used for the fixed frequency, the combination of switched capacitors and open-loop comparators can be used to achieve better resolution [2]. The most advantageous topology (high speed, small circuit area) will be chosen for the comparator design.

### 6.5.1 Open-loop

Open-loop comparator uses the amplifier stages (open-loop) to perform the comparison of two input signals. The optimum number of stages can be determined if the comparator is modelled

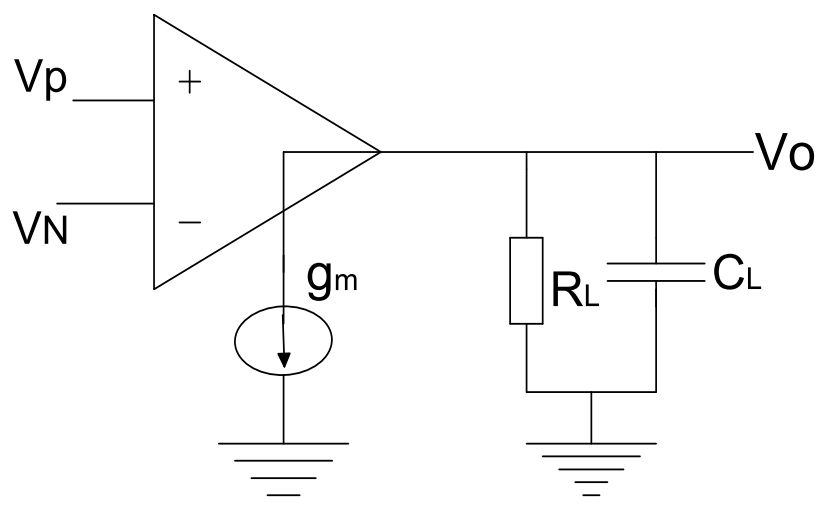


Fig 6.5.1: Comparator model

If  $t \ll T = RLCL$ , then the output can be approximated with  $V_a = gmRLVin(1 - e^{-t/(RLCL)}) \approx Vin \cdot t$ . It can be noticed that speed is increased by increasing the gain  $Av = gmRL$ . In order to decrease the propagation time delay, the chain of identical stages can be used. Under the same assumption, output voltage can be expressed as,  $V_a = Vin(1 - e^{-gmRLt})^n$ , where  $n$  is the number of

$n$  stages. For a given gain, the optimum number of stages can be found,  $Av^n = (n+1)^n$  and the propagation time delay  $t_{pn} = (n+1) \cdot t_p$ . Single amplifier has a limited capability and

normally a gain of maximally 10 times can be achieved. For example, if the gain is  $\sim 3$ , then the optimum number of stages is 6.

However, this optimum will require a large circuit area and three stages with the gain of 6 time (per stage) will provide equally good results with less circuit area. This means that a trade-off must be made between the circuit size and performance.

### 6.5.2 Regenerative

Regenerative type of converters (latches) uses the positive feedback to detect small differences between two voltages. The resolution is one of the key requirements which determine the power dissipation of the total comparator circuit. A stand-alone latch cannot be used for high resolution comparison since it exhibits large offset voltage ( $\sim 100\text{mV}$ ). Therefore, the latch will need one or more pre-amplifying circuits depending on the requirements. The use of pre-amplifying circuits will lead to a decrease in the power efficiency.

### 6.5.3 Open loop Regenerative

In the case that the regenerative circuit is not able to satisfy the design requirements, the combination is made, where the open-loop amplifier and latch are used, as shown in *figure 3.16*. In order to improve the comparator resolution, the preamplifier is used. It is followed by the latch circuit and the output buffer. This type of comparator will improve the comparator functionality in terms of propagation time delay and resolution.



Fig 6.5. II: Comparator that combines open-loop amplifier and latch circuits

## 6.6. Comparator\_design

In this chapter, the comparator design approach is presented. For high frequency circuit operation, the trade-off must be made between *speed* and *power dissipation*. Speed will be mainly influenced by the slew-rate requirements and the load impedance. The lower the

load resistance (or higher the load capacitance), the more current will be needed to achieve a desired speed of operation. The *gain* of the comparator will influence the speed and power dissipation. The gain per stage that can be obtained is limited. The total gain can be increased by inserting more stages, but this method has one disadvantage, namely the unacceptable circuit size. The gain could also be increased by increasing the *power supply voltage*. However, the maximal power supply is limited by the chosen technology. The *input impedance* of the comparator should ideally be infinitive, but is often capacitive and must be also taken into slew-rate analysis. The low *output impedance* is important concerning the (minimal) power dissipation within the last stage. In figure 6.6 the coherence between all of these design requirements is illustrated

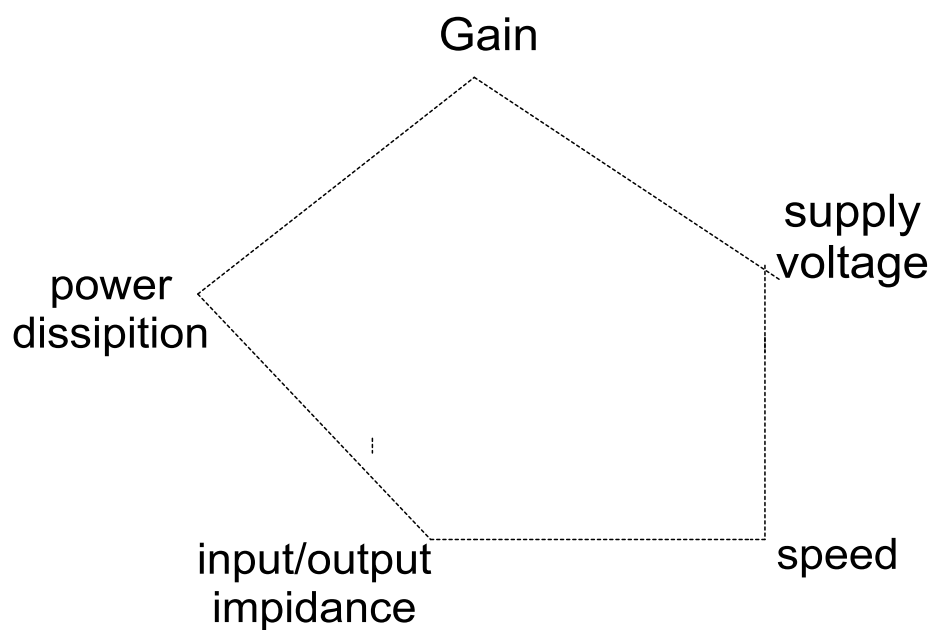


Fig 6.6: The design trade-offs

# **CHAPTER 7**

## ***Proposed comparator analysis and simulation***

## 7.A Circuit diagram and operation

Preamplifier Circuit Preamplifier is used to avoid kickback noise. It is implemented using differential pairs shown in Fig. The output of the preamplifier circuit is given to the back to back inverters which act as a positive feedback circuit and amplifies the feedback signal to achieve a decision. Depending upon the input and reference voltage. Here the incoming signal from back to back inverters gives a high or low signal .three non-overlapping clock signals are used and given as in the figure no 7.a.2

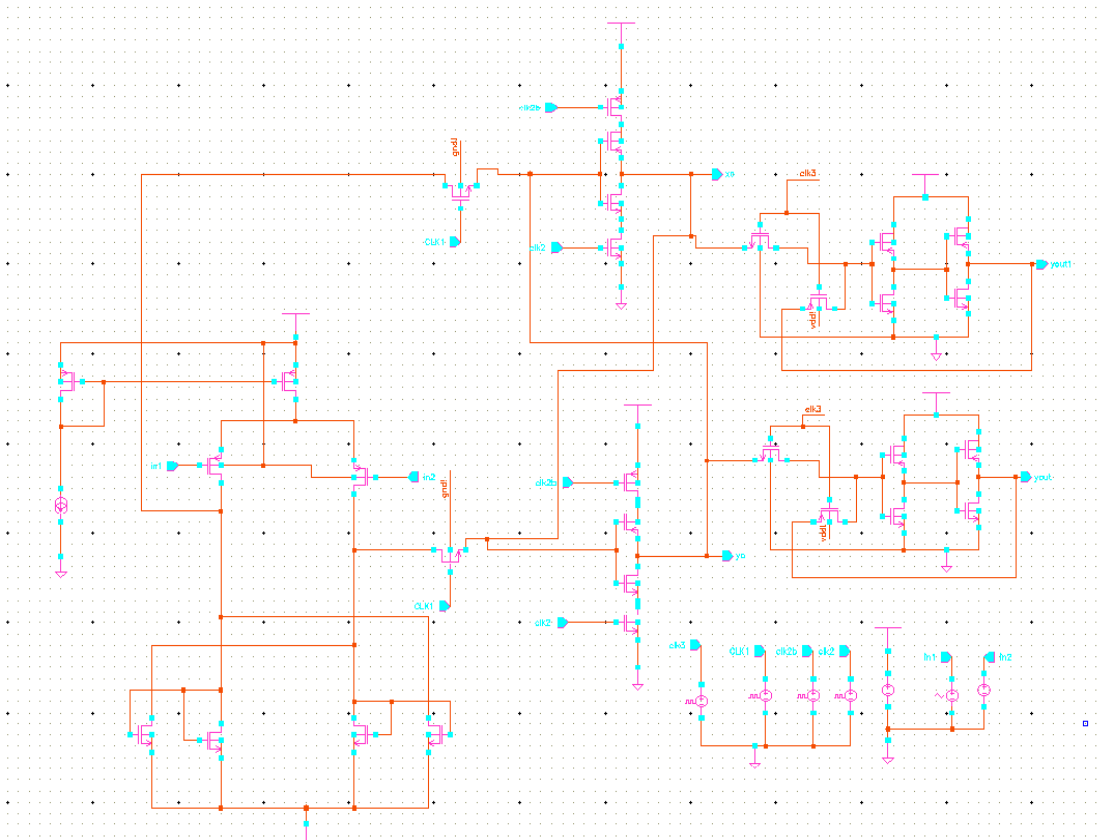


Fig 7.A.1 schematic of proposed comparator

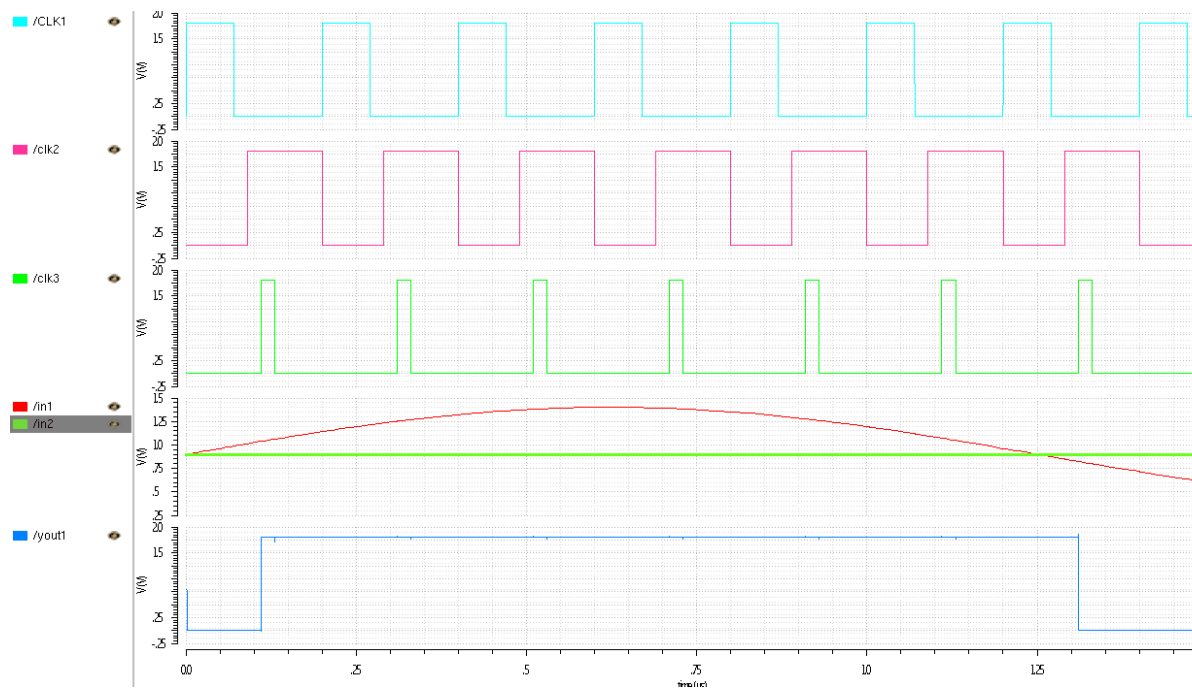


Fig 7.A.2 clocking mechanism and input/output

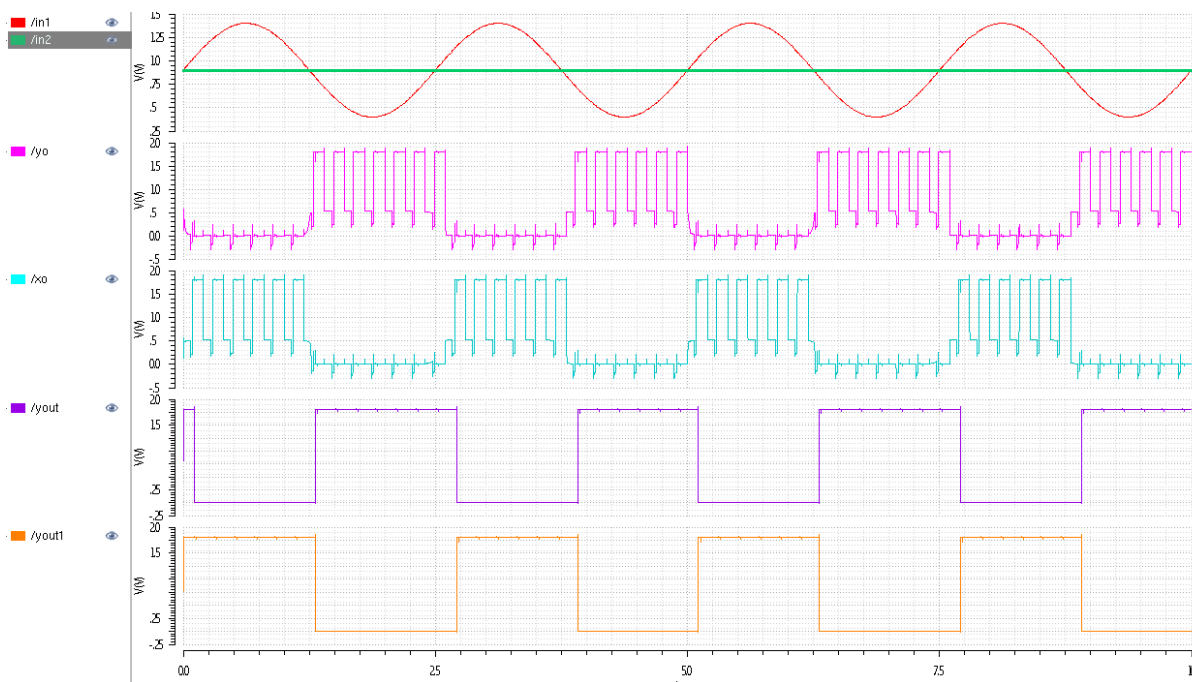


Fig7.A.3 transient response





7.A.4 power plot of proposed comparator

## **Result and discussion**

Power=21.79uW

## 7. B Modified pre-amplifier:

### 7.B.1 Circuit diagram and operation:

Preamplifier Circuit Preamplifier is used to avoid kickback noise. It is implemented using differential pairs shown in Fig. The output of the preamplifier circuit is given to the back to back invertors which act as a positive feedback circuit and amplifies the feedback signal to achieve a decision. Depending upon the input and reference voltage. Here the incoming signal from back to back invertors give a high or low signal. There are 3 non overlapping clock signals required. The use of extra two transistor is to isolate upper part of preamplifier from regeneration circuit .Rest operation is same as previous one explained.

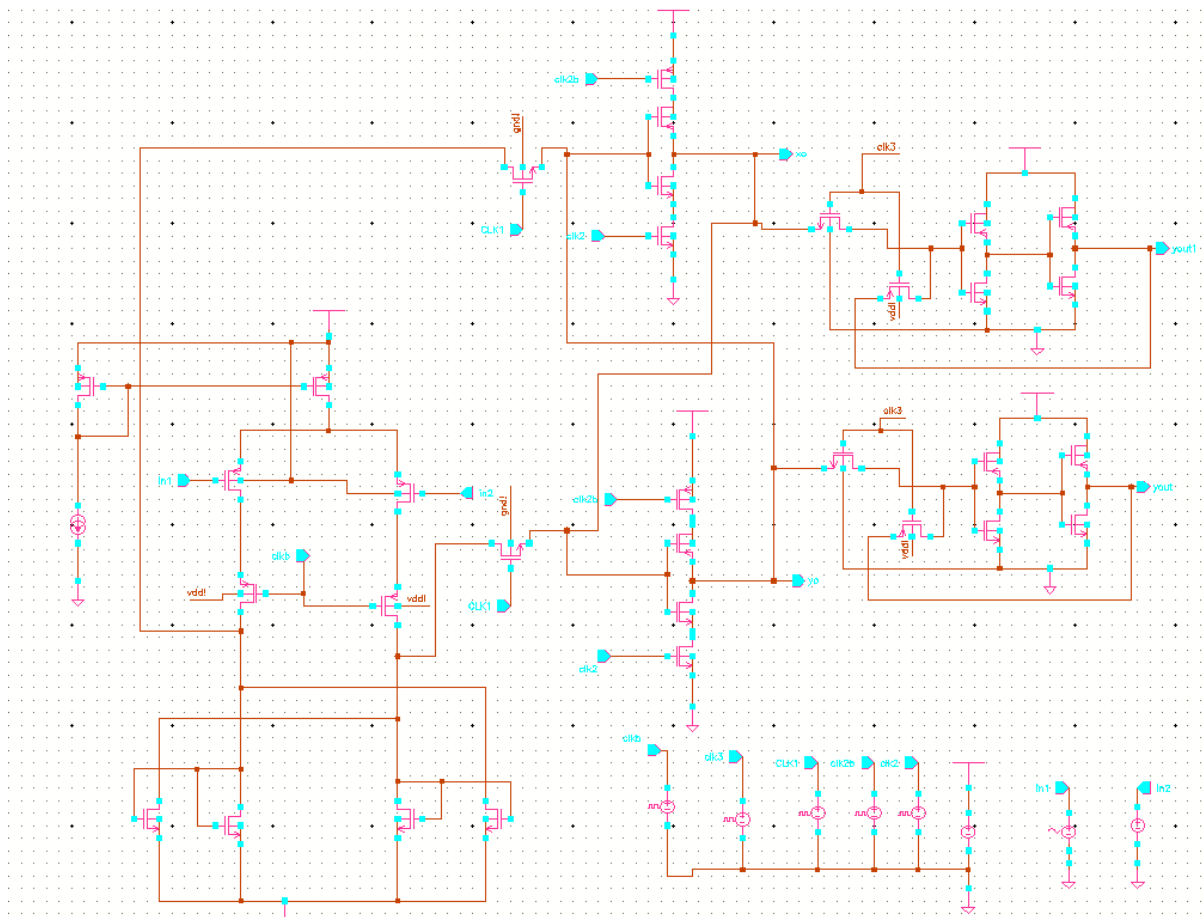


fig 7.B.1 schematic diagram of transistor

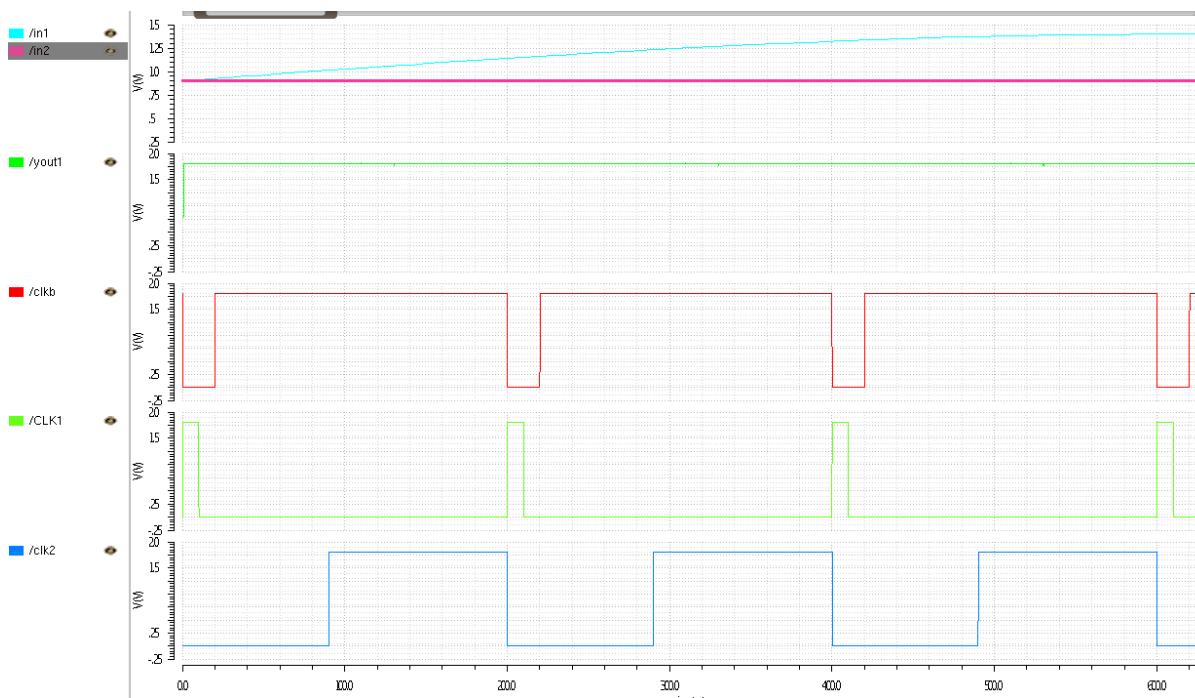


Fig 7.B.2 clock mechanism and input

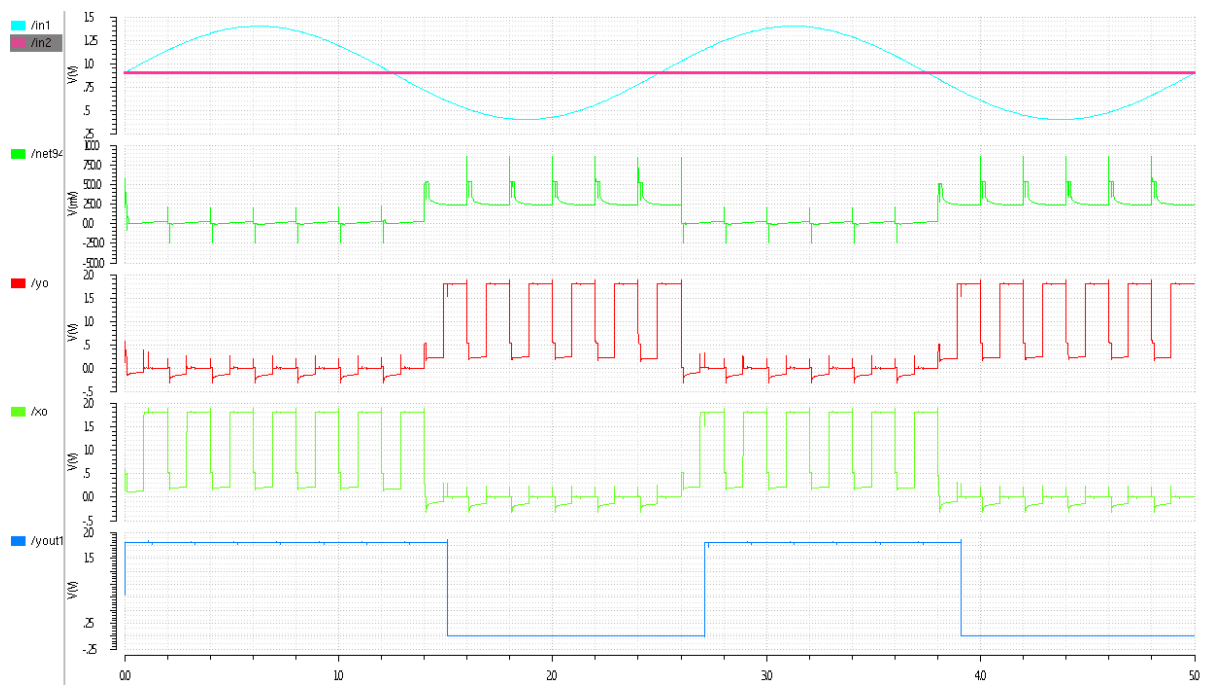


Fig 7.B.3 transient analysis

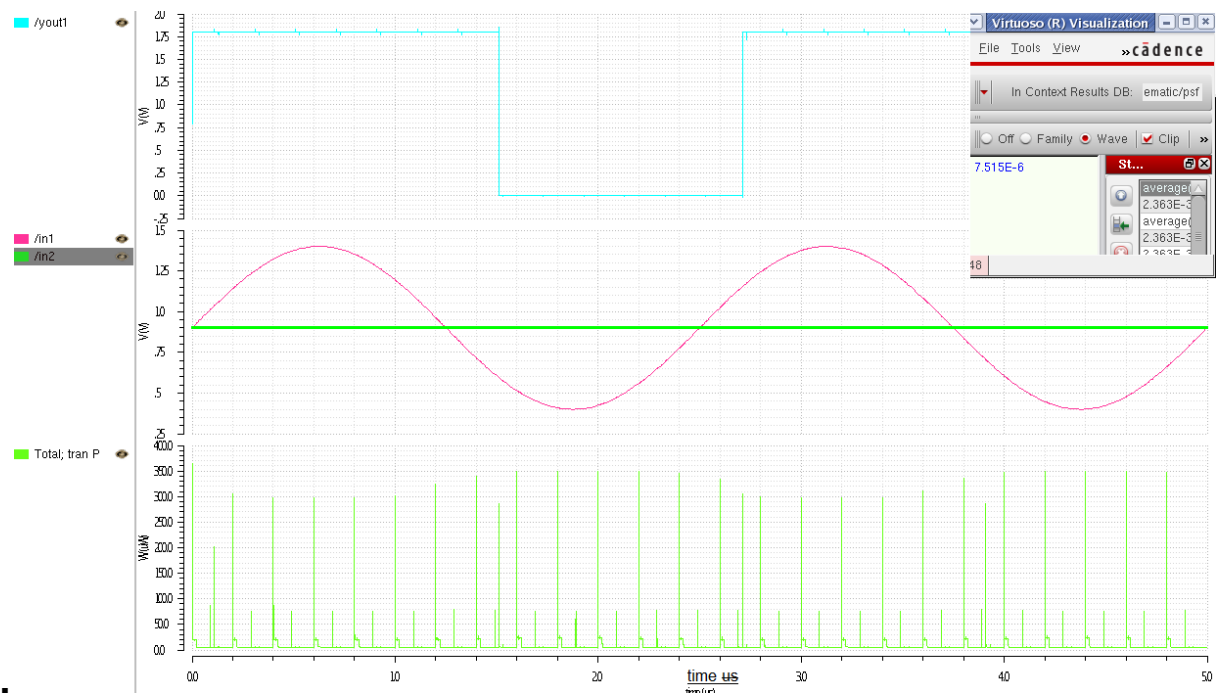


Fig7.B.4 power of proposed comparator

## Result and discussion

Power=7.5uW

## 7.C D-Latched dynamic comparator

### 7.C.1 Circuit diagram and operation:

**Fig 7.c.1** shows the dynamic latch comparator with preamplifier when the clock signal *en* goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M13 between the two cross coupled inverters. When *en* goes low the circuit enters the comparison phase. Transistor M8 is connected to the voltage supply and M4 is connected to ground. The transmission close and the comparator enter the regenerative phase. The output is a d-latch used to make the decision.

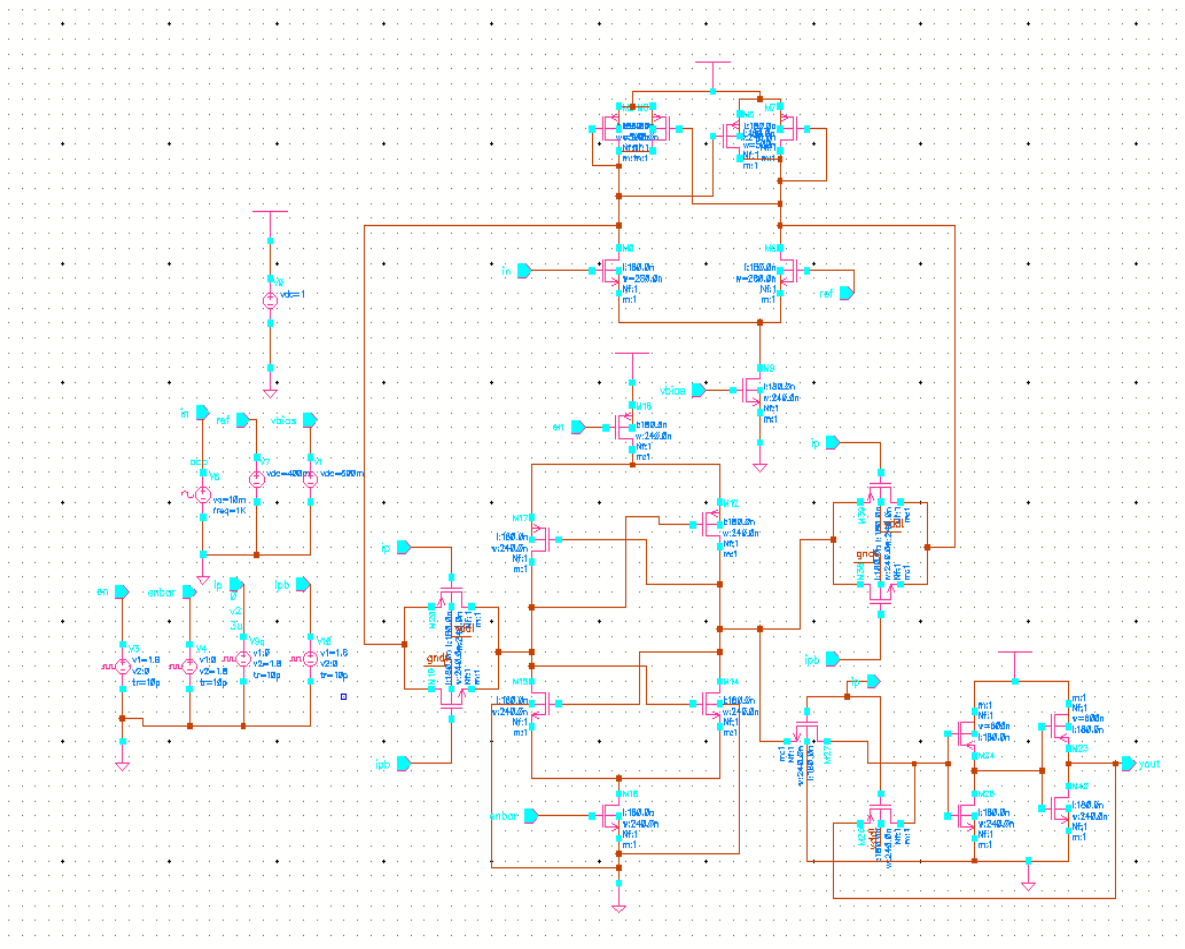


fig 7.C.1 schematic diagram of proposed comparator

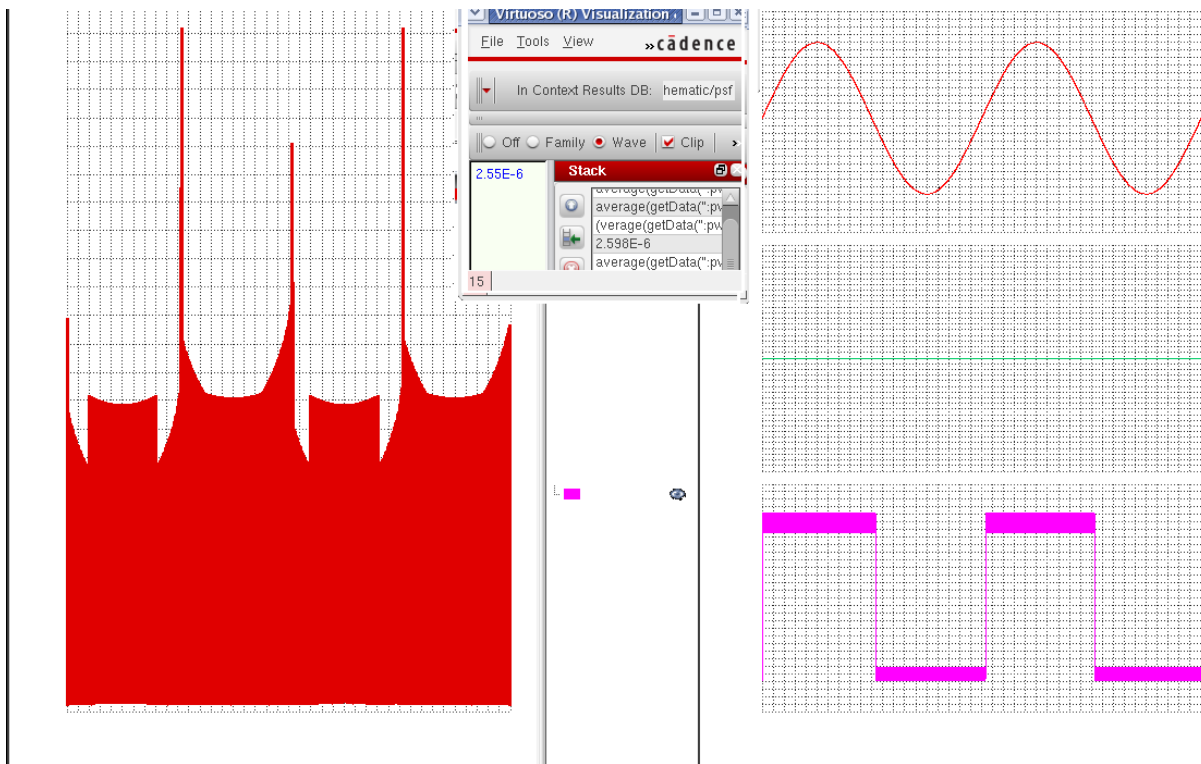


Fig7.C.2 power and transient of proposed comparator

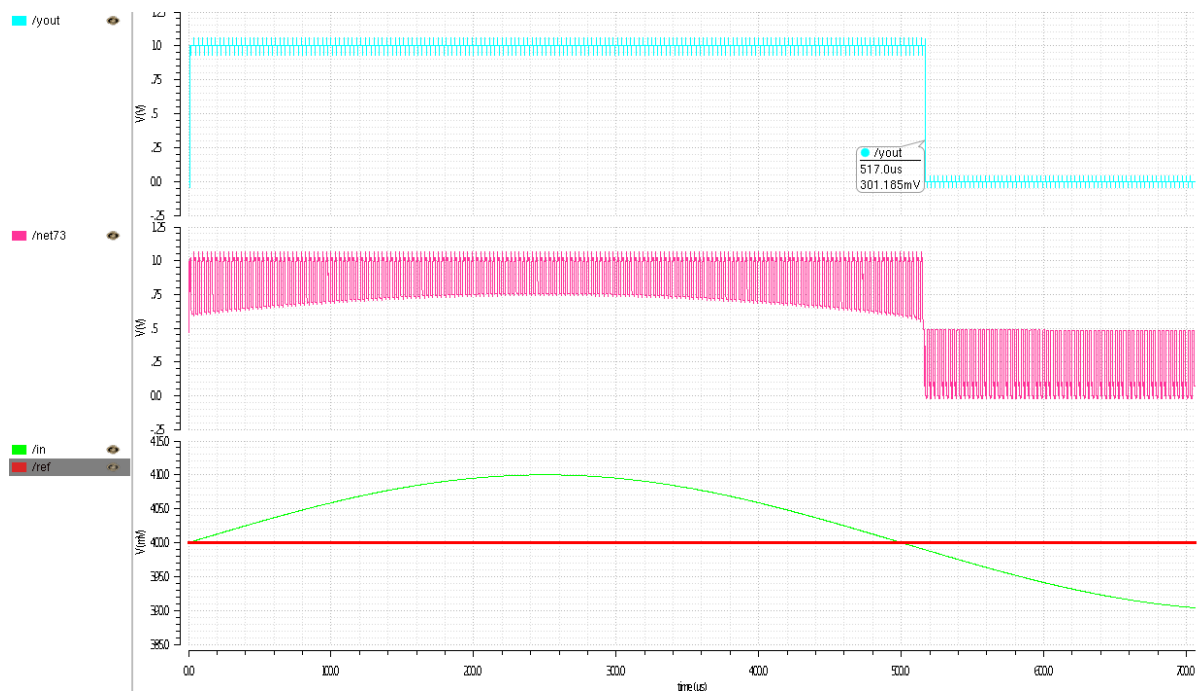


Fig7.C.3 Delay calculation

## **Result and discussion**

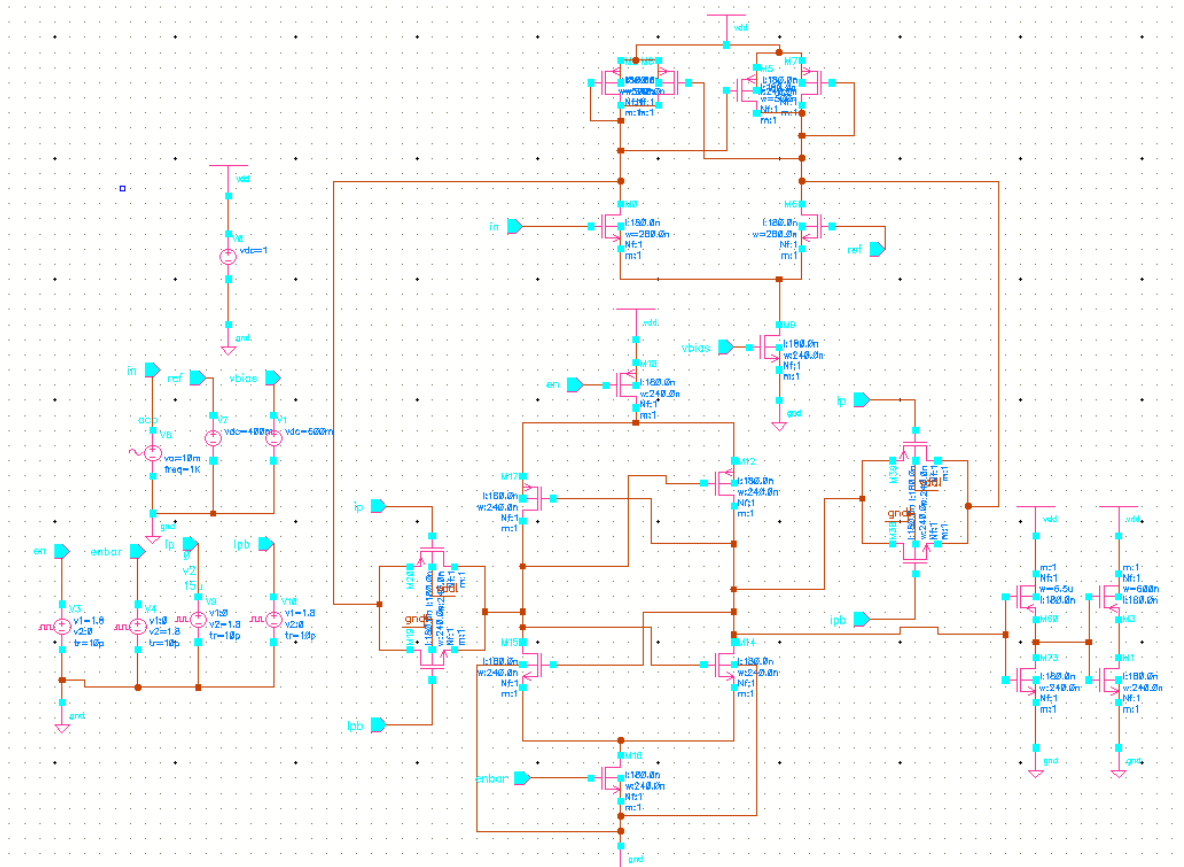
Power=2.55uW

Delay =17uSec

## 7.D Output buffer based comparator

### 7.D.1 Circuit diagram and operation

Fig7.d.1 in below shows the dynamic latch comparator with preamplifier when the clock signal en goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M13 between the two cross coupled inverters. When en goes low the circuit enters the comparison phase. Transistor M8 is connected to the voltage supply and M4 is connected to ground. The transmission close and the comparator enter the regenerative phase. Here the out put is taken from a buffer and rest is as previous section



7. D.1\_schematic diagram of Output buffer based comparator



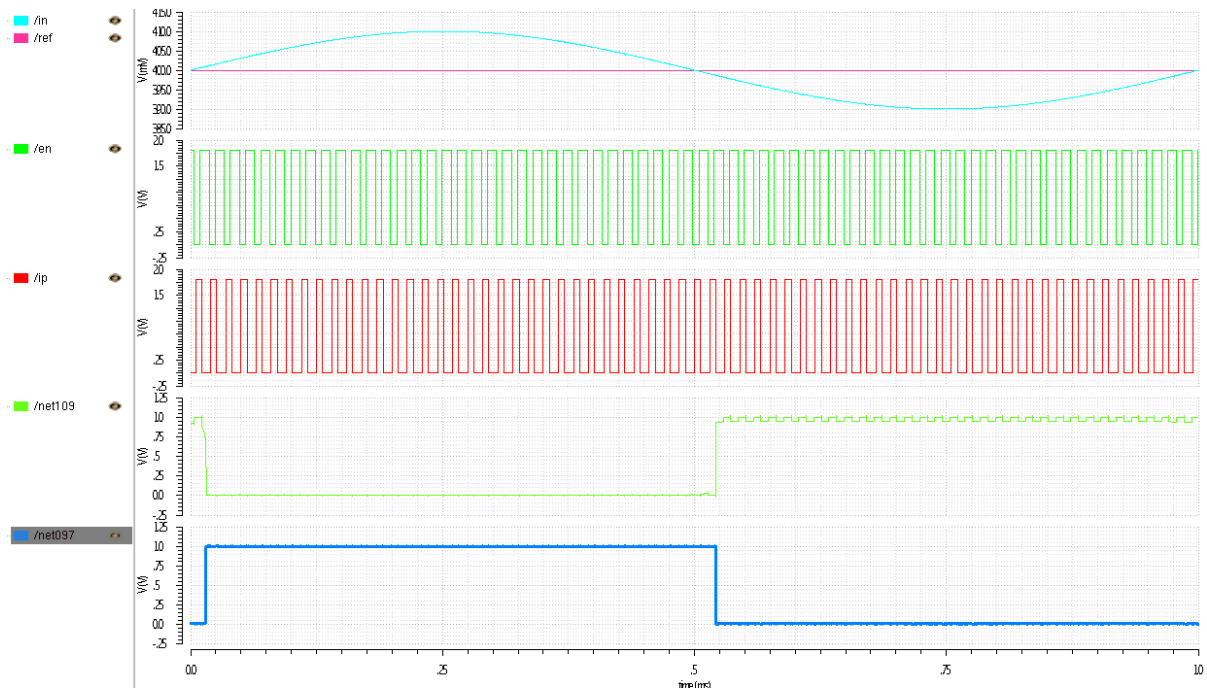


Fig 7.D.2 Transient analysis

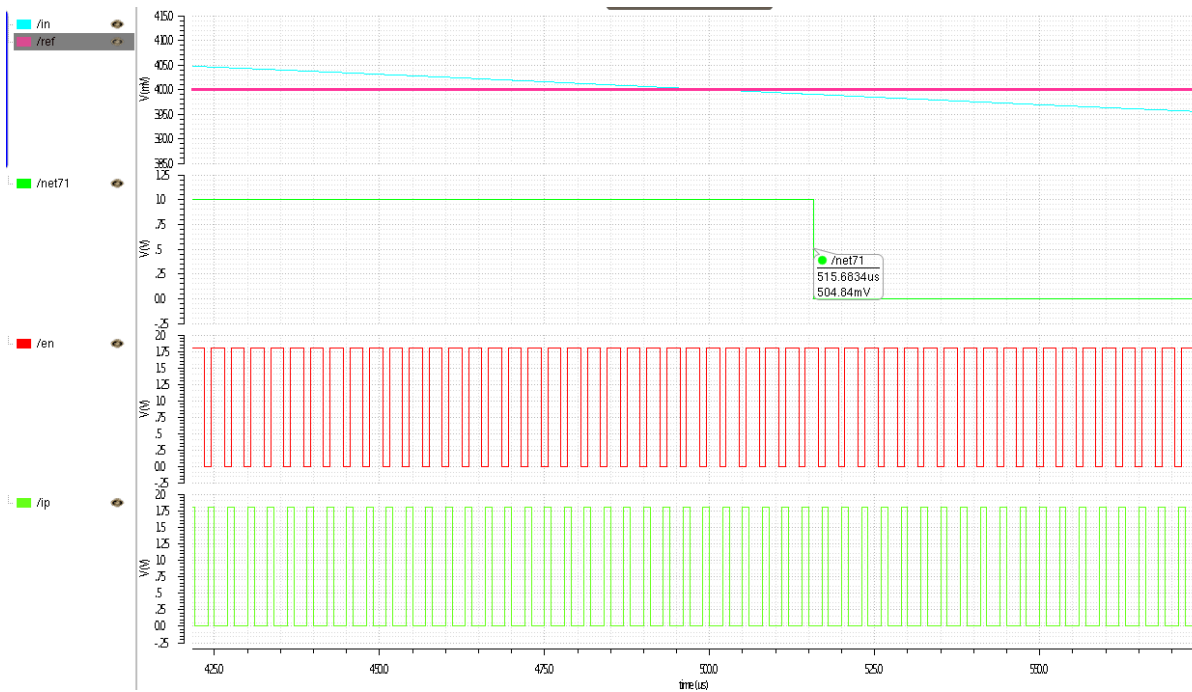


Fig7.D.3 Delay calculation

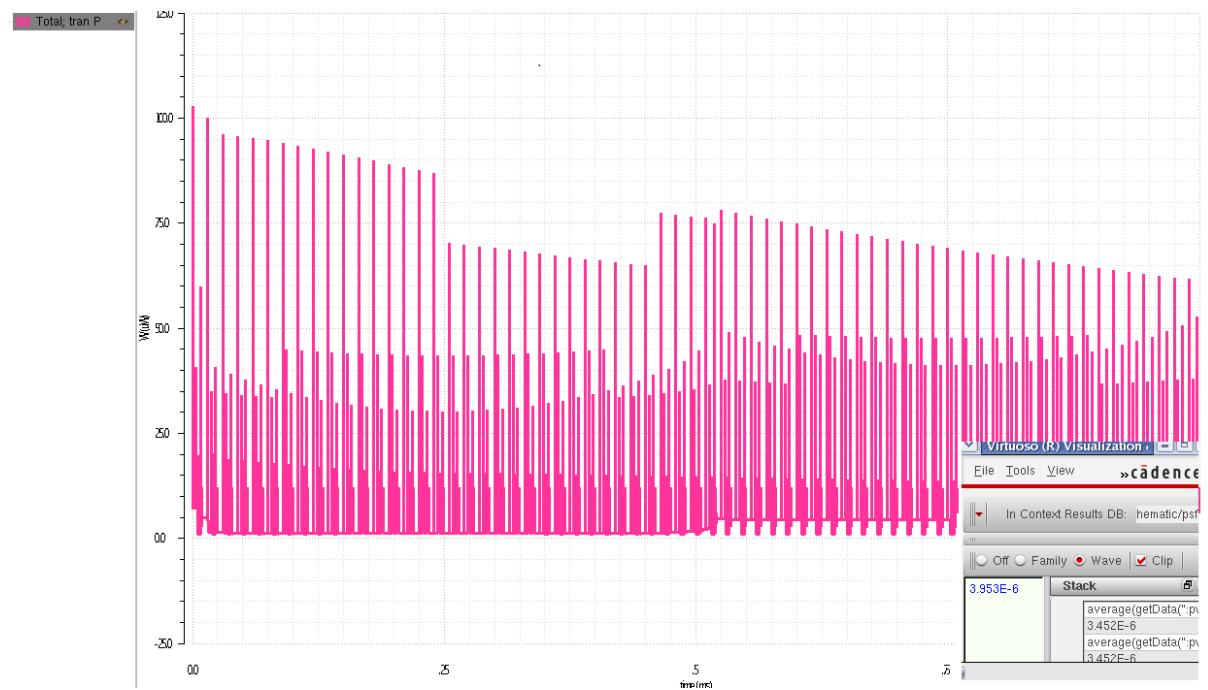


Fig7.D.4 power of Output buffer based comparator

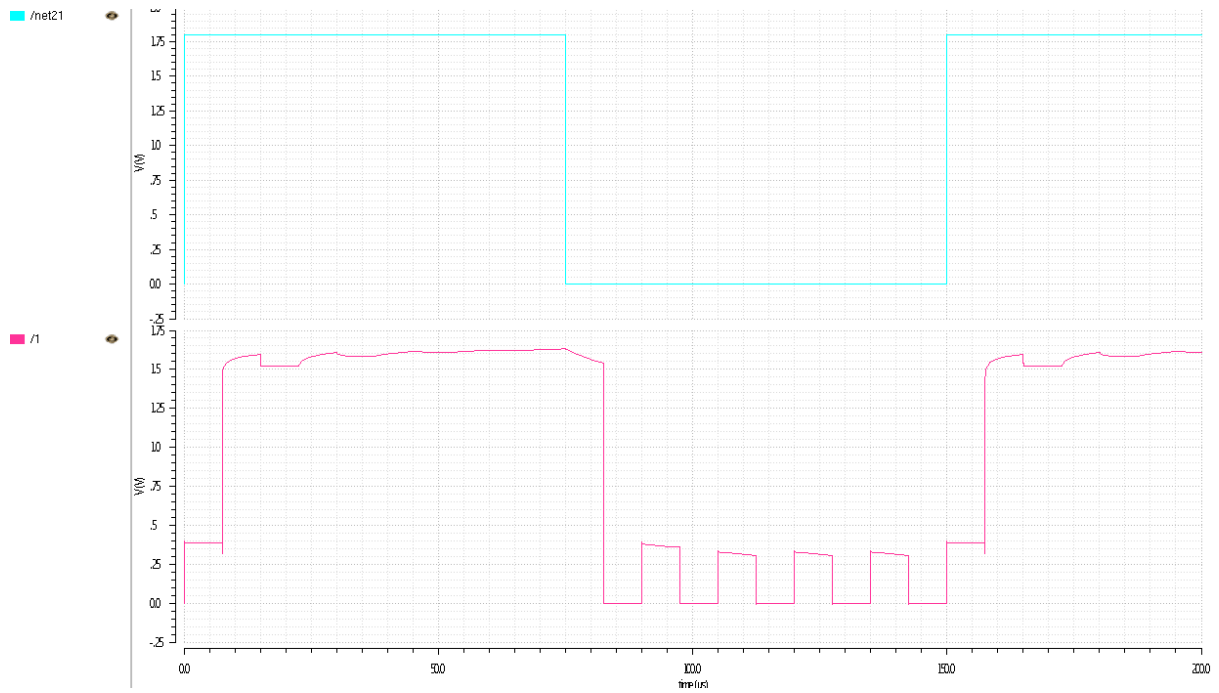
## **Result and discussion**

Power=3.95uW

Delay=15uSec

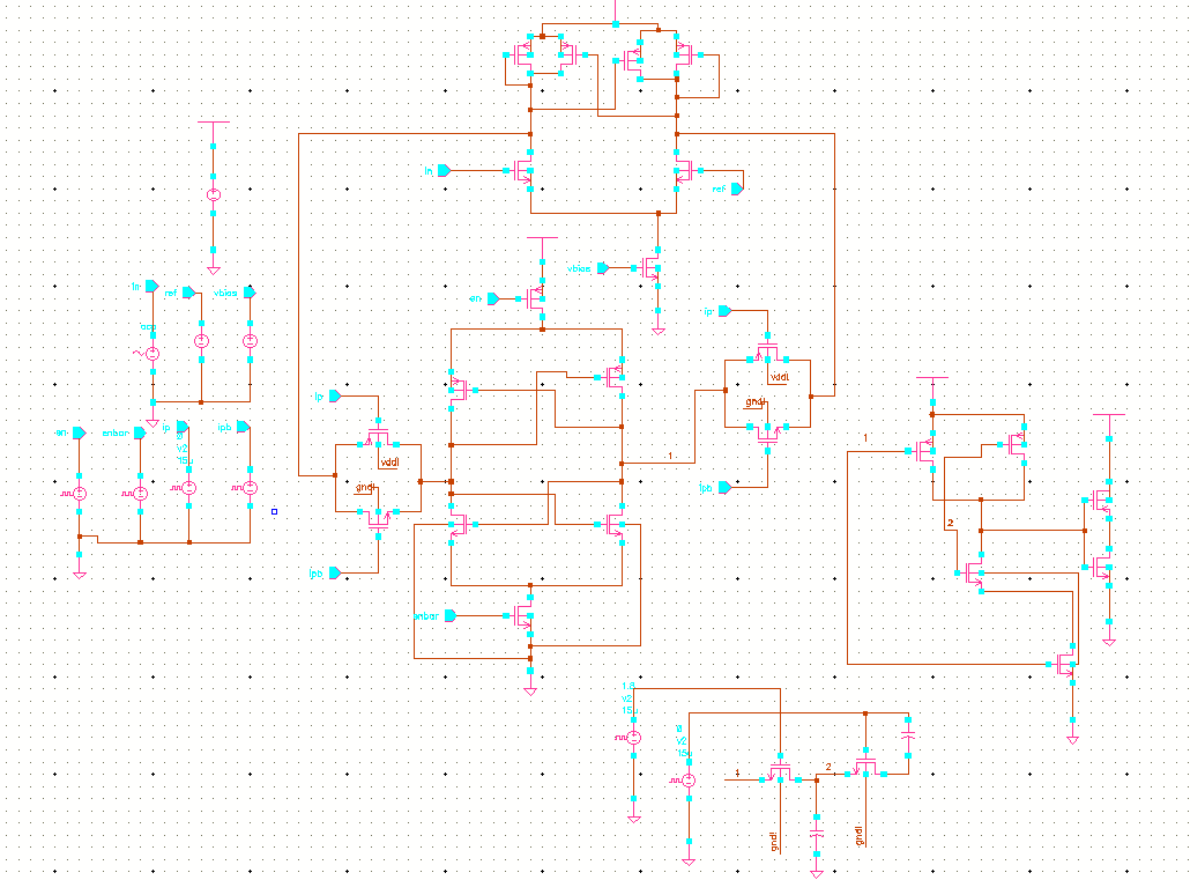
[illegible]

## 65



7E.2 Delayed wave form

## 7. F. Bucket delay model (BDM)



### 7. F.1\_schematic diagram of Bucket delay model (BDM)

Fig in below shows the dynamic latch comparator with preamplifier when the clock signal en goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M13 between the two cross coupled inverters. When en goes low the circuit enters the comparison phase. Transistor M8 is connected to the voltage supply and M4 is connected to ground. The transmission close and the comparator enter the regenerative phase. After the regeneration phase the signal is applied to BBD circuit and a delay is obtained and then both the signals are passed through a AND gate to get a perfect square wave.

Wave form

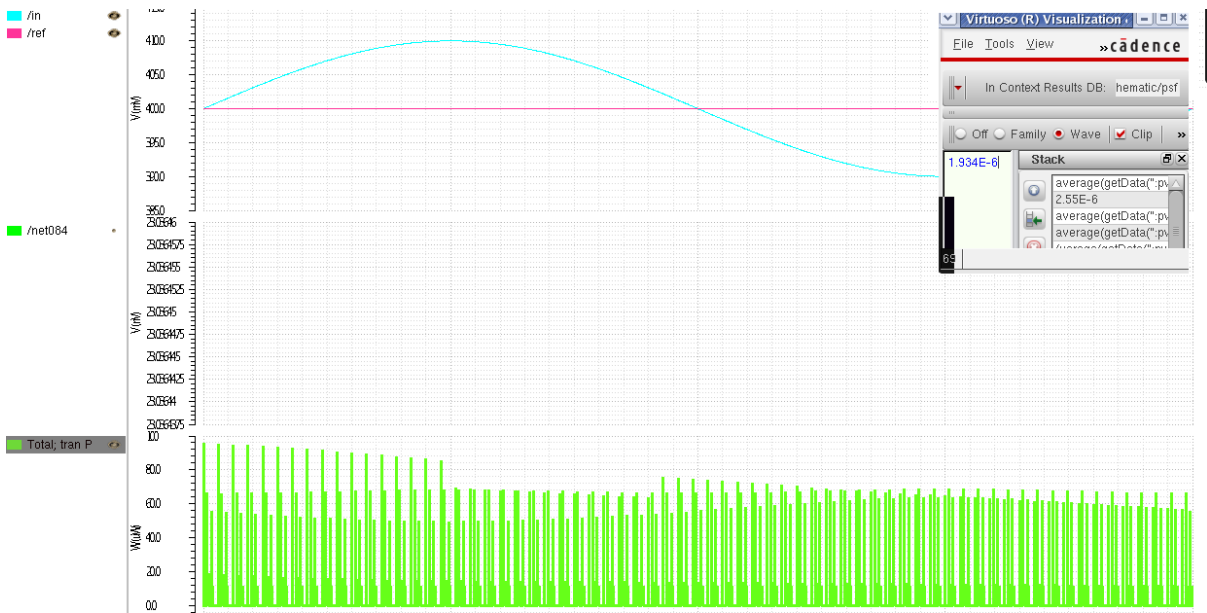


Fig7.F.2 power of Bucket delay model (BDM)

Result and discussion

Power=1.93uW

## Conclusion

The above proposed comparators were designed and simulated using cadence GSPDK 180nm technology and proposed 1,2 show less power 21.9, 7.5  $\mu$ W respectively, with VDD 1 volt. Among pre amplifier based comparators BBD showed the lowest power 1.93  $\mu$ W and also less delay. Depending upon technology requirement the appropriate design can be chosen.

## Future work

From simulation result one can design for low power circuit the performance improvement can be done using auto zeroing technique and kick back noise should be minimised and for the study of hysteresis can be done. On an average the future work can be any one among these.

- Accuracy (dynamic and static offset, noise, resolution)
- Settling time (tracking BW, regeneration speed)
- Sensitivity/resolution (gain)
- Meta stability (ability to make correct decisions)
- Overdrive recovery (memory)
- Power consumption

# Appendix

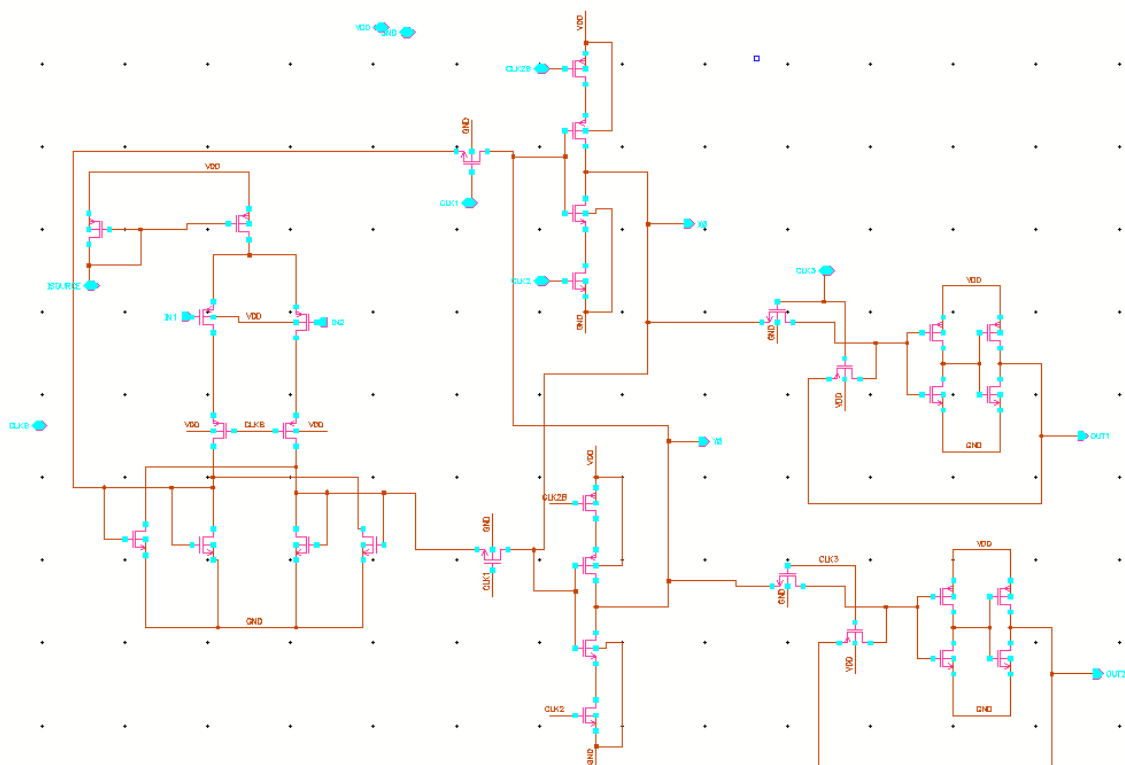
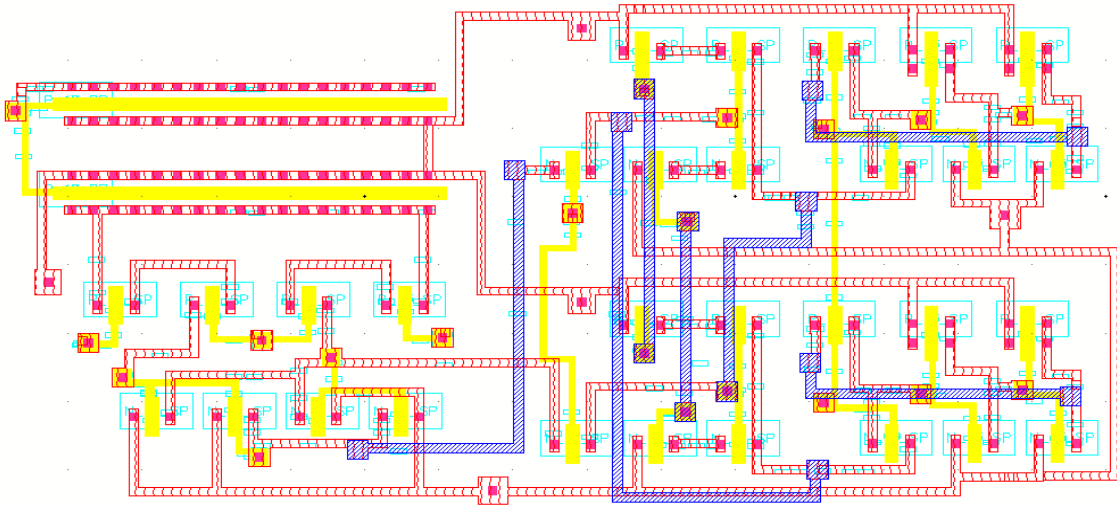
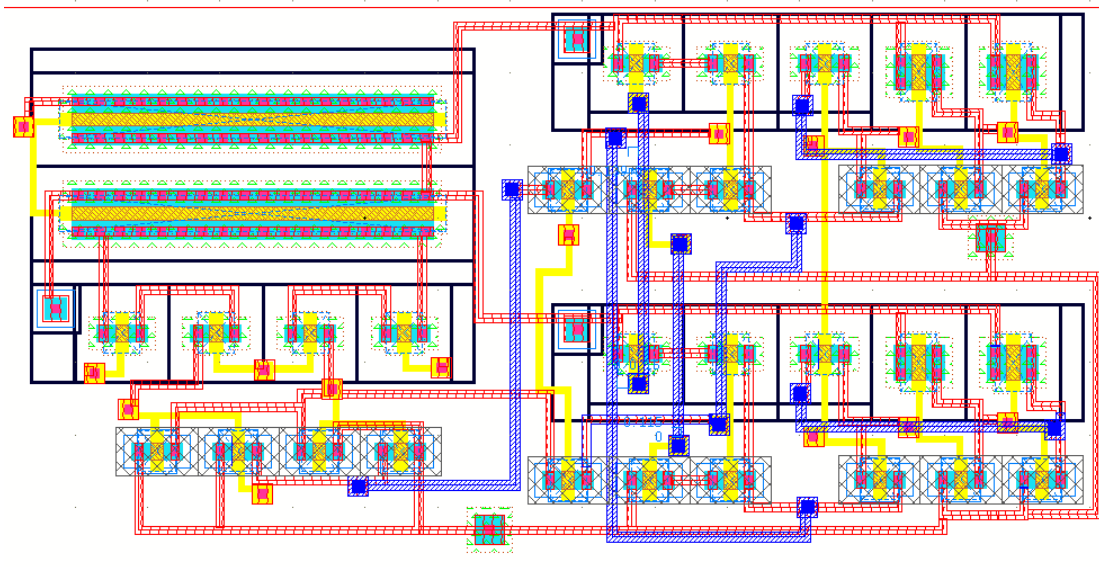


Fig A: schematic of improved pre amplifier based dynamic comparator





**Fig B:** Layout of improved pre amplifier based dynamic comparator



**Fig C:** AV extracted of improved pre amplifier based dynamic comparator

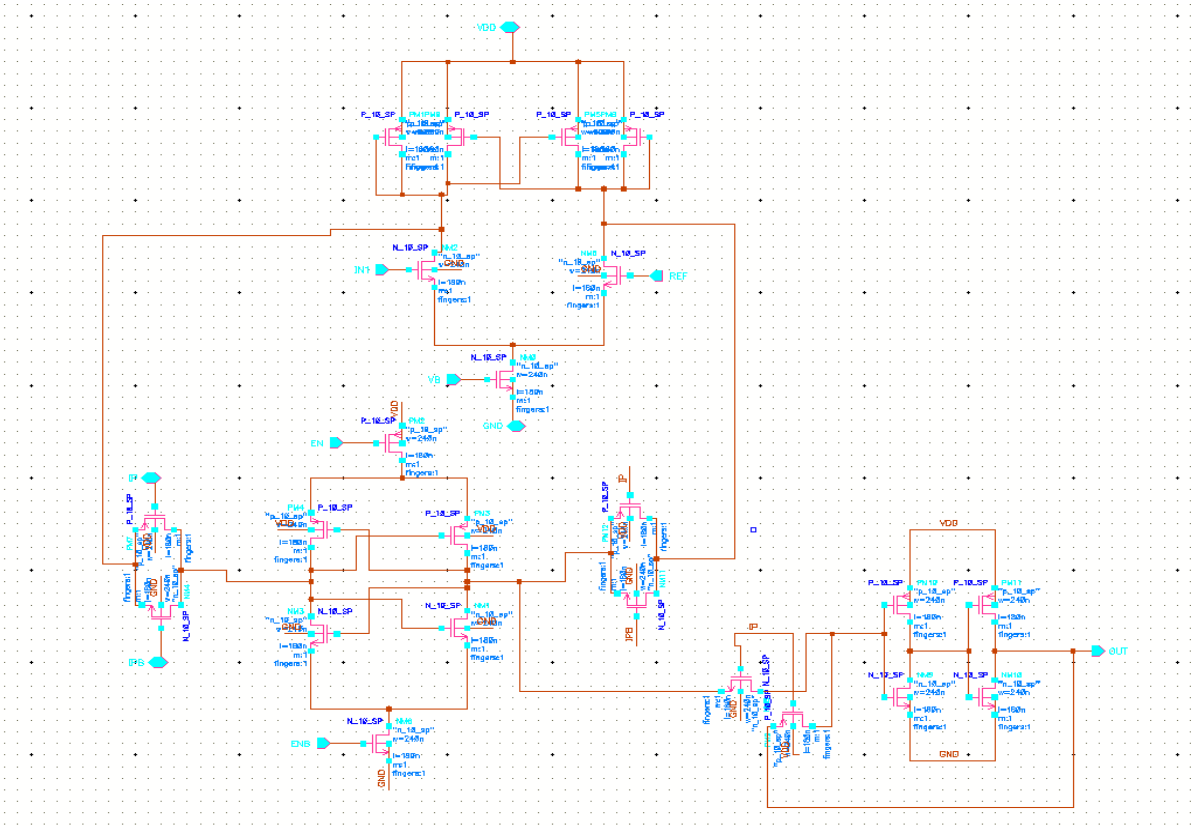


Fig D: d latched based comparator

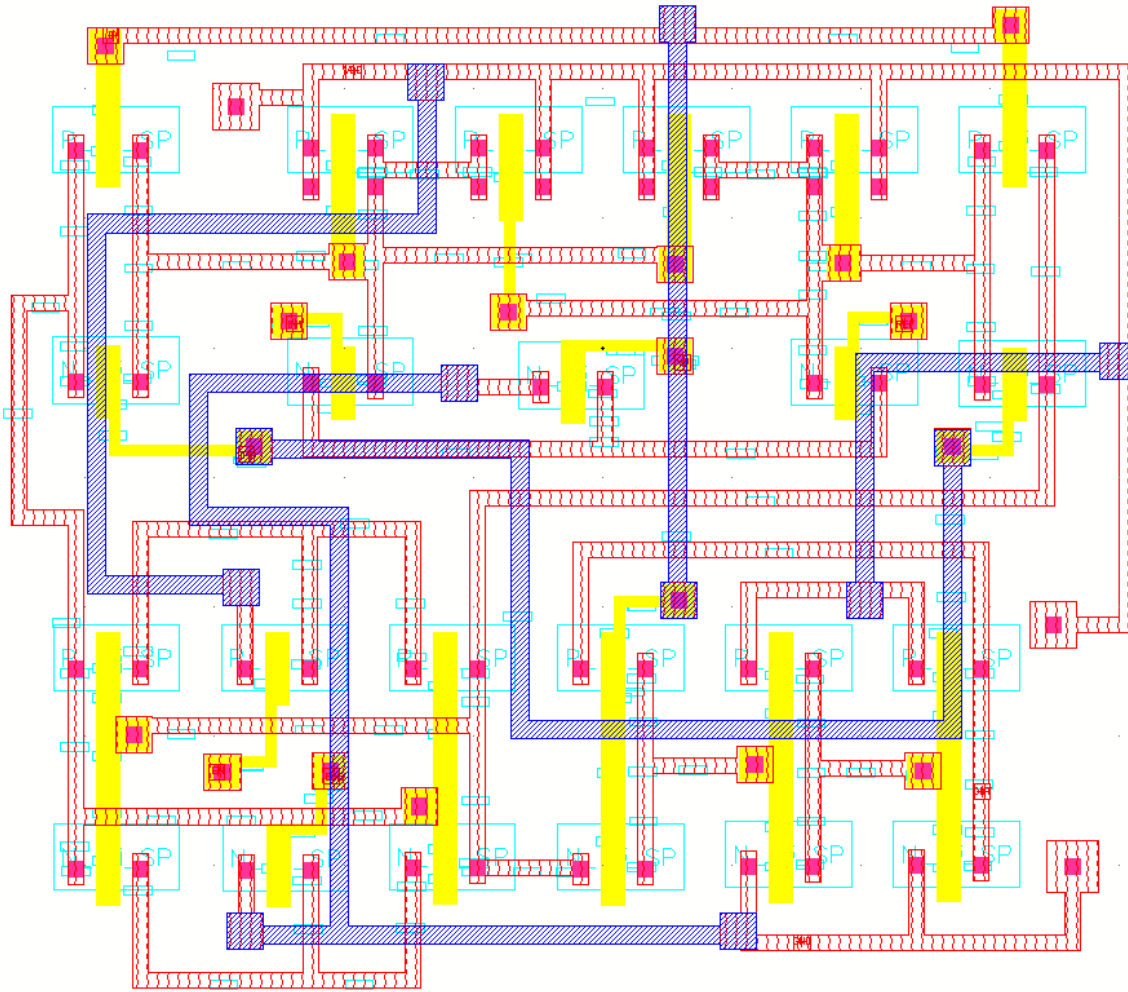


Fig E: layout of D latched based comparator

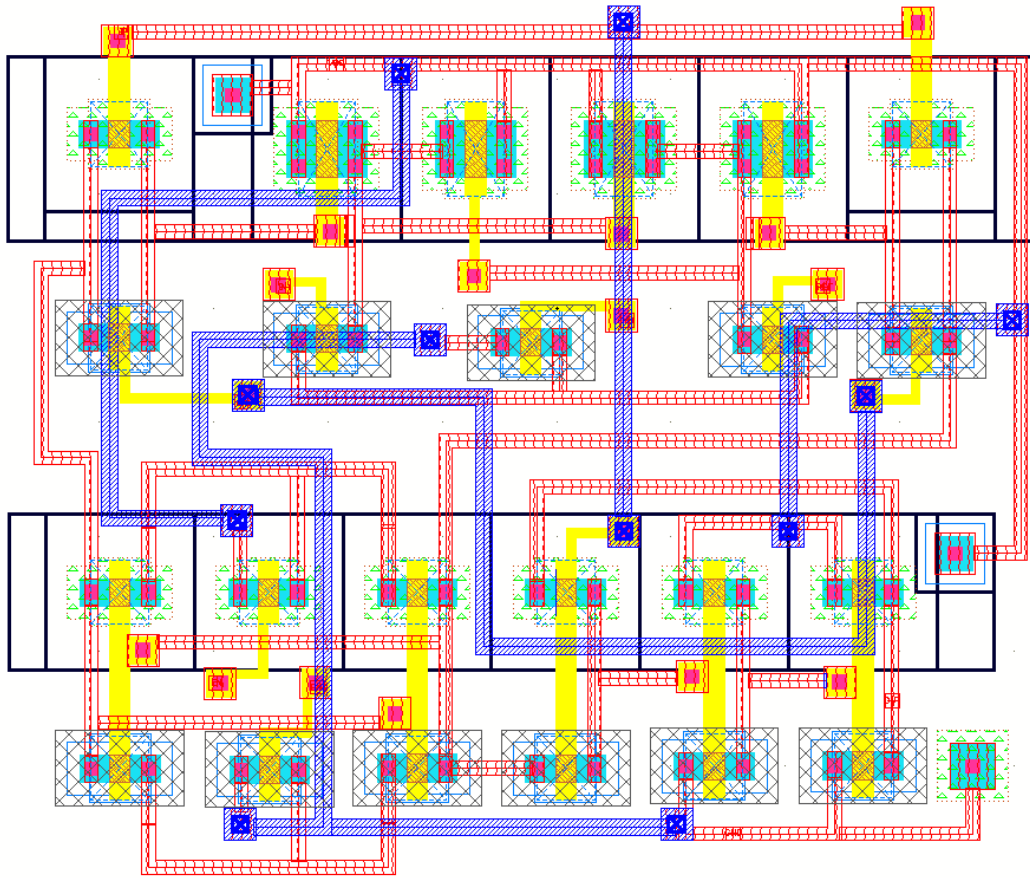


Fig F: AV extracted view of buffer comparator

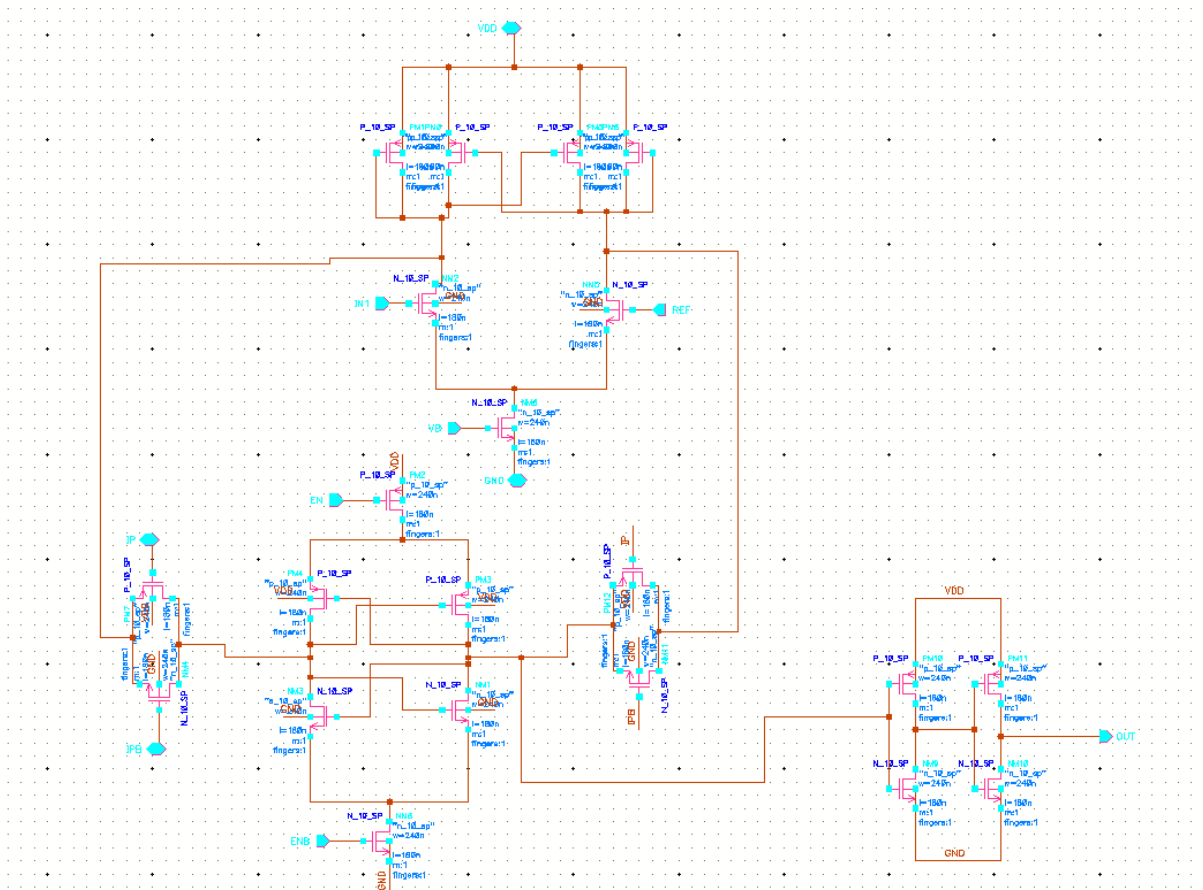


Fig G: schematic of buffer based dynamic comparator

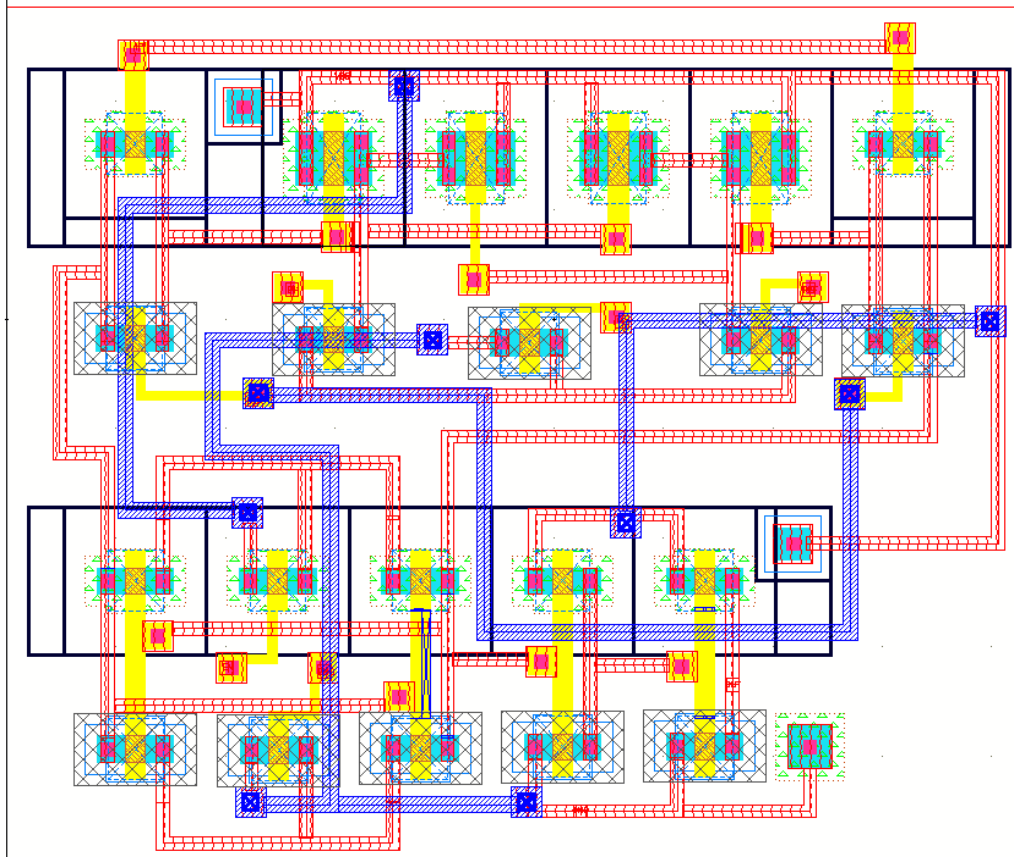


Fig H: AV extracted of buffer based dynamic comparator

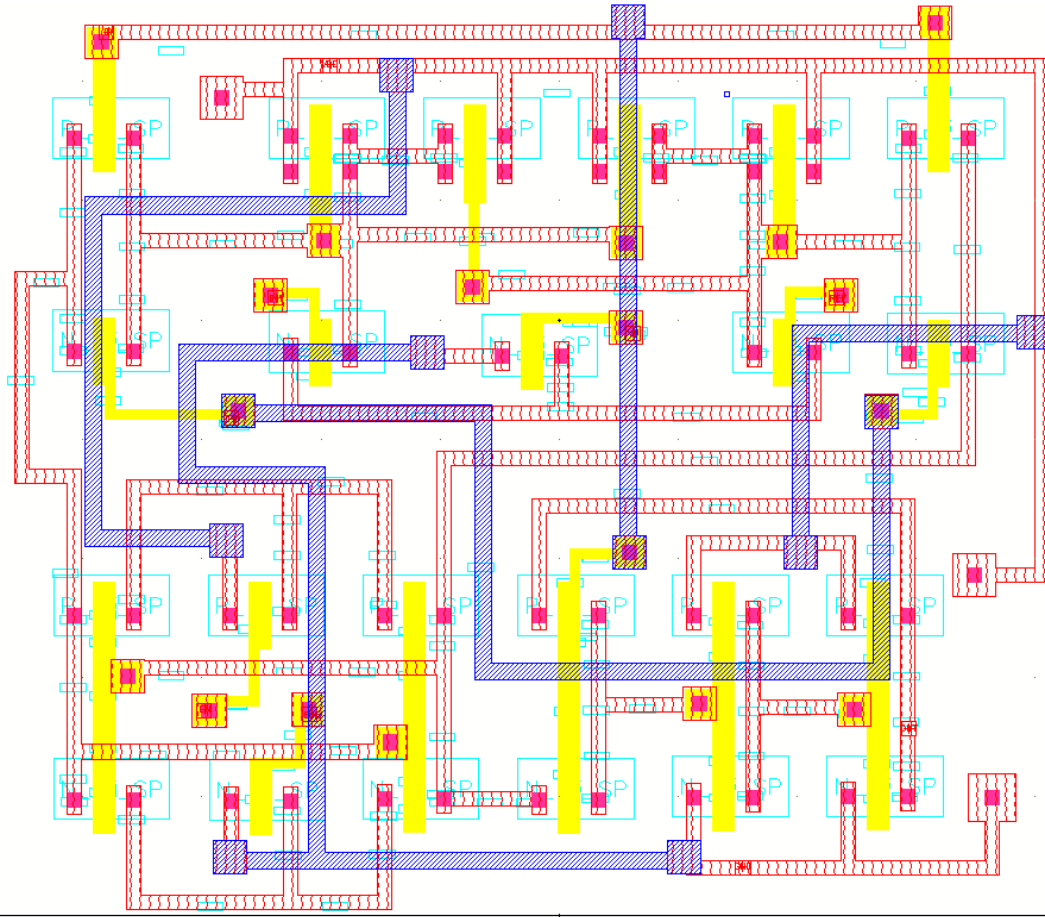


Fig I: layout of buffer based dynamic comparator

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